AMD
Vitis

5 PRODUCTIVITY-BOOSTING BENEFITS OF THE AMD VITIS™ HLS TOOL FOR HARDWARE DESIGNERS

AT A GLANCE

Experience intuitive design, rapid verification, and simplified retargeting of adaptive SoCs and FPGAs. The AMD Vitis high-level synthesis (HLS) tool helps you bring high-performing designs to market—fast.

1 GET OUT OF THE CODE AND INTO RAPID FUNCTIONAL SIMULATION

Simulate and verify designs in a fraction of the time

The Vitis HLS tool enables you to tap into a higher level of abstraction—leveraging optimized libraries and C-based test benches for early validation, debugging, and functional verification while reducing the need for iterations during the hardware design phase.

Video designs, for example, can be simulated as full frames in a fraction of the time of traditional RTL design. The tool also allows for co-simulation of the HLS C code in conjunction with the RTL portion of the design.

2 FIND THE OPTIMAL RTL IMPLEMENTATION—FAST

Explore and compare design options before finalization

A variety of optimization directives and pragmas are included within the Vitis HLS tool to help you meet your target design performance.

You can use the tool's code analyzer feature to view performance estimations, visualize the potential for task parallelism, and identify the architectural changes needed to optimize performance before running C-synthesis. Once C-synthesis is completed, a summary report provides insight into timing, performance, resource use, and more.

3 DESIGN, ITERATE, THEN ITERATE AGAIN—IN RECORD TIME

Work productively in high-level C/C++ code

The Vitis HLS tool empowers you to work in C/C++. You can change parameters (such as base frequency or video resolution) in C code and let the tool do the conversion to RTL, reducing complexity and the opportunity for error. Additionally, you're able to reuse existing C/C++ functions, increasing design productivity.

You can make changes quickly in response to simulation results, performance metrics, or other feedback within the tool—before regenerating RTL. Now you can focus on the algorithms without getting bogged down in hardware intricacies.

4 OPTIMIZE FOR NEW USE CASES USING PRE-DEVELOPED FUNCTIONS

Leverage a large set of HLS libraries to build designs

The Vitis HLS tool comes with a robust set of library functions you can instantiate that are optimized for AMD adaptive SoC and FPGA architectures. This makes it easier than ever to build custom designs for unique applications.

5 DESIGN LARGE SYSTEMS WITH SIMPLE TOOL INTEGRATION

Use powerful AMD design tools in conjunction

Moving between different design stages is simple with the Vitis HLS tool. Create your custom IP and functions using the tool, then integrate them into the AMD Vivado™ Design Suite or the AMD Vitis™ Model Composer to build a complete design.

Now you can develop heterogeneous designs for AMD adaptive SOCs and FPGAs with ease and speed using powerful, complementary software solutions spanning the complete design flow.

CAPTURE INCREASED PRODUCTIVITY WITH THE AMD VITIS HLS TOOL

Simplify adaptive SoC and FPGA hardware design and work more efficiently with the Vitis HLS tool.

Learn more about how you can accelerate design closure and speed time to market.

Download the Vitis HLS tool today to get started.