Solutions for the DSP Market

Presenter

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Xilinx UK
Solutions for the DSP Market

Agenda

• Zooming in - The Xilinx Device Range.
• Concepts - Brief Overview of the Xilinx FPGA Architecture.
• Algorithms - What are the requirements of DSP?
• FPGA's vs DSP Requirements - A closer look at the XC4000E
• Tradition - The limit of DSP processors.
• Back to basics - building the right blocks.
• Solutions - Some case studies from Europe.

**Xilinx Components Today...**

- **LOW COST**
  - XC8100
  - XC7200A
  - XC7300

- **HIGH SPEED**
  - XC3000A
  - XC3100A

- **DESIGN METHODOLOGY**
  - XC5200
  - XC4000

- **DENSITY**
  - XC5200
  - XC4000E & XC4000EX
  - XC4000
  - XC3000A
  - XC2000
  - XC9500

RAM Based Multiplier for FPGAs

Xilinx High Density FPGAs

- **XC3100A FPGA Family**
  - Highest speed solutions

- **XC5200 FPGA Family**
  - Cost Optimized, high volume production solution

**XC4000E & XC4000EX FPGA Families**

- Highest speed, Performance Optimized

**Speed**
- System Performance to 100MHz
- High speed extension to XC3000A
- Full PCI Compliance

**Density**
- VersaRing™ I/O Flexibility
- Dedicated arithmetic logic
- System Perf. to 50MHz

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FPGA Architecture

Configurable Logic Blocks

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RAM Based Multiplier for FPGAs

Configurable Logic Block (CLB)

- Function Generators
  - Implement GATES of design
  - Can be used as ROM
  - Various RAM Options
  - Combine with Carry Logic to form many Arithmetic functions

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Flip-Flops
- Optional use
- Clock enable available
- ZERO hold time

Carry Logic

Configurable I/O Block (IOB)

- Three-State Buffer
  - Optional
  - Bus signals
  - Open Collector

- Passive Pull-up & Pull-down
  - Optional
  - 50-100K Ohm

- Pad
  - Many package Types
  - Sink 12mA
  - TTL & CMOS
  - Slew rate Control
  - Soft start up
  - IEEE 1149.1 Boundary Scan

- Polarity control
  - on data and controls

- Flip-Flops
  - Optional use
  - Clock enable available
  - ZERO hold time

KC & PH (Xilinx) June 1996
**Programmable Interconnect**

- Resources to create arbitrary interconnection networks
- Hierarchy of interconnect resources
- Programmable switches
- Internal 3-state buffers for busses, mux's, and wide functions
- Dedicated global clock networks
- Global reset and tri-state networks

**FEATURES**

- **Master mode**
  - ‘Self Configuration’ from PROM
  - Parallel (shown) or serial modes
- **Peripheral mode**
  - Dynamic reprogramming via external system (microprocessor)

**BENEFITS**

- Field Upgrades via Software Changes
- Built-in System Test/Diagnostic Logic
- Adaptable System Design
  - Hardware changes & tuning possible during prototype AND OPERATION!
- Examples
  - Separate Read/Write Logic - Tape Drive
  - Evolving Communications Protocols
Algorithms:
What are the requirements for DSP?

There are really only 4 functions:
- DELAY
- ADDITION/SUBTRACTION
- MULTIPLICATION
- DATA STORAGE

Question becomes: How BIG and how FAST can these be implemented in an FPGA?

FPGA Architectural Requirements

<table>
<thead>
<tr>
<th>Operation</th>
<th>Preferred Feature</th>
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<tr>
<td>Delays</td>
<td>Register Intensive Part. FIFO Capability.</td>
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<tr>
<td>Addition / Subtraction</td>
<td>Built-in Arithmetic Capability</td>
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<td>- Improves speed &amp; reduces logic area.</td>
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<td>Multiplication</td>
<td>Fast Arithmetic Capability On-Board RAM/ROM</td>
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<td>Data Storage</td>
<td>On-Board RAM/ROM</td>
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RAM Based Multiplier for FPGAs

XC4000E Architectural Features

Features:
- Register Intensive Parts
  - Clock Enable to ALL Flip-flops
  - Asynchronous Set/Preset to CLB Flip-flops.
- Fast Built-in Carry Logic
  - Fully Reconfigurable.
- Select-RAM
  - High Speed.
  - Synchronous & Asynchronous modes.
  - Single & Dual Port Operation
  - Configurable RAM Content.

Advantage to DSP:
- Pipelining & Data Delays
  - East system level I/O
  - >2000 Flip-flops (XC4025E)
- Arithmetic Functions
  - Fast Addition / Subtraction
    - 16-bit Add = 17ns (-3)
  - Fast Comparators
  - Multipliers
- Data Storage & Delays
  - Coefficient Tables.
  - Cyclic Buffers.
  - FIFO’s.
  - Multipliers
- Sizable to Application

XC4000E Select-RAM™ Memory Advantages

Select the Size
- No wasted resources
- Scalable to needed size
- MEMGEN software
  - Automatically generates RAMs of specified size.

Select the Function
- Can be Single or Dual Port
- Synchronous or Asynchronous
- “Mix and match”

Select the Location
- Can be located anywhere on die
- Adjacent to critical circuits for speed

Select the Programming Method
- Via Bitstream on start-up
- During design operation
**Tradition - The limit of DSP Processors**

**Very Good Devices**
- Microprocessor Architecture.
- Special Multiply and Accumulate Instruction.
- On chip memory for program and data.
- Programmed by software.
- Instruction times down to 12ns (80MHz).

**Limitations**
- Fixed Architecture.
- Fixed bit sizes.
- SEQUENTIAL processing.

**Typical DSP Device Architecture**

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**Traditional Sequential Processing Limits System Performance**

Where do FPGAs fit on this graph?
Traditional Sequential Processing Limits
System Performance

Sample Rate
MSamples/s

Number of Operations per Sample

Where do FPGAs fit on this graph?

DSP Algorithms are Parallel

FIR filter

\[ D_{\text{out}} = \sum_{n=0}^{\infty} k_n t_n \]

Implementation Method                  Requirements                  Performance
Sequential (Traditional DSP)           ONE full function multiplier  LOW
Parallel (Distributed Arithmetic)      Multiple Constant Coefficient multipliers  HIGH
Building the right Blocks

**DELAY**

2-Bits per CLB

32-Bits per CLB

**ADDITION/SUBTRACTION**

MULTIPLIERS

These require a little more effort......

All Functions expand to SIZE REQUIRED at point in Algorithm

MULTIPLICATION - Typically 4 Methods

**ADDER TREE**

Fast (8-Bit - 65MHz)
Large (8-Bit - 68CLB)

**LOOK-UP TABLE**

A ROM is pre-programmed with all possible answers

**SHIFT & ADD**

Compact (8-Bit - 20CLB)
Slow (multi-cycle)
8MHz SYSTEM performance may be high!

**LOGICAL TREE**

A huge exercise in Boolean Algebra!
Each bit out is an equation of the inputs.

Can be Fast Complex & Very Large

RAM Based Multiplier for FPGAs

KC & PH (Xilinx)  June 1996
Method 5 - The Hybrid Multiplier

Constant (k) Coefficient Multiplier (KCM)

Effectively performs a **HEXADECIMAL** multiplication

Implements: \( Y = k \times X \)

8-Bit Version
Compact 20 CLB - Same as **SHIFT & ADD**
Fast (66 MHz) - Same as **ADDER TREE**

Implementation of Look-Up Tables

Fixed Constant
(variable by configuration!)

Variable Constant !

**What is required?**

- Option to use ROM and yet still ‘tune’ value by ISP
- Ability to choose RAM if required
- Ability to build RAM of exact width required
- Ability to build RAM/ROM exactly where it is needed on the die
- Ability to build as many blocks of memory as required
- Ability to preset an initial value on configuration
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Performance of KCM’s
Results for the fully available -3 speed grade ( -2 speed offering ~14% improvement)

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Figures are worst case and measured IN-SYSTEM

Defines the upper SYSTEM performance and size for Xilinx DSP Solutions
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8-Bit MACs/XC4025-3

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**Sample Rate**

MSamples/s

10 20 30 40 50 60 70 80

**Number of Operations per Sample**

10 20 30 40 50 60 70 80

Defines the upper SYSTEM performance and size for Xilinx DSP Solutions

8-Bit MACs/XC4025-3 10-Bit MACs/XC4025-3

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**XILINX**

KC & PH (Xilinx) June 1996

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**DATE 11/11/96**

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**Performance of KCM’s**

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Defines the upper SYSTEM performance and size for Xilinx DSP Solutions

- 8-Bit MACs/XC4025-3
- 10-Bit MACs/XC4025-3
- 16-Bit MACs/XC4025-3

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**Real Solution 1 - 55MHz Low Pass Filters**

**XC4013-3**

**Application**
- Front end filters for Measurement Equipment.

**Requirement**
- Each filter required 6 taps FIR (symmetrical) with 10-bit data and coefficients.
- Sample rate of 55 Msamples/second.
- Coefficients to be fixed after initial system tuning phase.

**Solution**
- Single device solution offering 30% of device for additional system logic.
- Full parallel Processing - Equivalent to over 600 MOPs processing.
- Implementation performed completely by customer.
Real Solution 2 - 2.2MHz Bit-Filter/Correlator

Application
- Base-Station Communications Bitstream processing.

Requirement
- A 96-Tap FIR filter structure (symmetrical) with 16-bit coefficients
- Coefficients liable to modification during life time of design.
- Sample rate of just below 2.2 Msamples/second.

Solution
- Single device solution offering 22% of device for additional system logic.
- Slowest speed grade available - Higher data rates instantly available.
- Distributed RAM and ROM employed for samples and coefficients.
- Mixed Sequential and Parallel technique - Equivalent to over 200 MOPs processing.
- Basic Implementation performed by Xilinx.
- 16x clock utilized to perform 3 sequential processes in parallel.

Real Solution 3 - Data Routing & Sequencing

Application
- Communications Noise Reduction System (Spread channel communications).

Requirement
- Record 256-bit packets on four 2 MBit/s channels.
- Segment into 2-bit elements.
- Route any element to any output at any.
- Total control from uP.

Solution
- Single device solution.
- 11 blocks of RAM - total of 5760 bits.
- Implementation performed by customer and Xilinx.
- System requirements were evolving by the DAY and a 4 week time-scale.
Solutions for the DSP Market

Summary

• Zooming in - Large Xilinx Device Range for many applications and methodologies.
• Concepts - Xilinx FPGA Architecture offers a completely flexible approach to design.
• FPGA’s vs DSP Requirements - XC4000E offers the density and performance for DSP.
• Algorithms - Consider the algorithm structure to optimize the logic design (cost).
• Tradition - Sequential processing and fixed architectures limit system performance.
• Back to basics - Mastering the basics and asking the right questions about the algorithm.
• Solutions - 2MHz or 55MHz, Multiplication or Data Manipulation, Flexible and Successful.

Try Xilinx

Solutions for the DSP Market

THANK YOU

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