Using FPGAs to Design Gigabit Serial Backplanes

April 17, 2002
Outline

• System Design Trends
• Serial Backplanes Architectures
• Building Serial Backplanes with FPGAs
Key System Design Trends

• Need for ....
  – Easy Scalability of Performance
  – Extremely High Availability
  – Flexible Architecture
  – Use of Standards
    • Rapid Time to Market
    • Reduces Costs
Merging Communications & Computers

- Communications Systems have serial backplanes
- Computers moving to serial backplanes

Database servers
Application servers
1U Web servers
Ethernet Switches

Internet

"Bladed Server", PICMG 2.16
Serial Standards

• Serial Standards
  – Fiber Channel 1 Gbps
  – Ethernet 1 Gbps
  – InfiniBand 2.5 Gbps

• Parallel Standards Going Serial
  – PCI => 3GIO
  – RapidIO => Serial RapidIO
  – ATA => Serial ATA

• Channel Bonded Serial Standards
  – XAUI 10 Gigabit Ethernet (4 x 3.125 Gbps)
Serial Connectivity = Higher Bandwidth & Fewer Pins

Example - PCI: 32-bit x 33MHz = 1 Gbps, Shared among 5 clients 250 total pins

Virtex-II Pro System: 2.5 Gbps x 4 x 5 = 50 Gbps 80 total pins

Each Client has 2.5 Gbps guaranteed to every other Client

50x higher bandwidth with less than 1/3 of the pins
Serial Link Rates

Link Rates (bits per sec.):
- 155M
- 3.125G
- 1.25G
- 622M
- 10G
- 40G
- 200G
- 1000G
- 4000G
- 7680G

Mainstream Deployment:
- OC-192
- Infiniband
- GigE
- OC-48
- OC-3
- OC-12
- FC
- FC-2x
- FC-10x
- 3GIO
- SxI-5
- Rapid IO
- OC-768
Serial Topologies

- Switched
- PICMG 2.16

- Full Mesh
- PICMG 2.2
- PICMG 3.x
Building Serial Backplanes with FPGAs

Gigabit Ethernet Phy x2

Gigabit Ethernet MAC x2

Switched

PICMG 2.16
Virtex-II Pro™ Platform FPGA

- Industry's Fastest FPGA Fabric
- Up to 4 IBM PowerPC™ Processors Immersed in FPGA Fabric
- Up to 16 Embedded Rocket I/O™ Multi-Gigabit Transceivers
- Up to 8 Digital Clock Managers
- On-Chip Termination with XCITE Technology
- Up to 216 Multipliers
Virtex-II Pro Rocket I/O™ Technology

Up to sixteen multi-gigabit serial transceivers
Support 622 Mbps to 3.125 Gbps full duplex operation
Flexible PCS/PMA feature set
**Xilinx® Rocket I/O Serial Backplane Interface Technology**

- Rocket I/O Serial Backplane Interface (RSBI) Technology
  - Simple solution for serial backplane applications
  - Consists of two parts
    - The RSBI/ “Aurora” link protocol
    - An RSBI Reference Design (IP core) implementing that protocol
RSBI/ “Aurora” Protocol

- An Efficient, Lightweight Protocol to Move Data Point to Point across Serial Link
- Used to transport higher-level protocols
  - Standard protocols like Ethernet
  - Proprietary, customer-defined, protocols
RSBI Core

- Implements RSBI/ “Aurora” Protocol
- Provides a simple interface for transferring packets across
  - A single gigabit serial link
  - Up to 16 bonded links
- Minimal Use of Resources (~350 slices)
- Frequency and Technology Independent
- Specifications and Source Code available from Xilinx
RSBI/ “Aurora” Features

• Uses 8B/10B and includes CRC protection
• Transmitter wraps user data in Rocket I/O “Aurora” protocol
  – Handles packet formation
  – Sends error notification to remote core
• Receiver recovers frames and realigns data
  – Strips packet/frame wrappers
  – Aligns data on double word boundary
  – Monitors error conditions
RSBI User Interface

User interface created so no knowledge of Rocket I/O block is necessary
RSBI Channel Bonding

• All lanes must have passed comma detect before channel bonding starts
• Uses same technique as 10 Gigabit Ethernet and Serial RapidIO
  – Sends semi-random IDLE pattern

Synchronization of individual channels into a single large data channel
RSBI/ “Aurora” Implementation Parameters

- Allows maximum frame size of 8K Unlimited bytes
- 32-bit internal interface
- Other frame sizes and internal interface widths planned in future releases
Error Detection in Hardware

• Errors can be either in Rocket I/O block or link(s)
• Five sources of link failure detected:
  – Link physical error threshold overflow
  – Channel misalignment
  – FIFO overflow
    • Receiver or transmitter
  – Transmitter sending an illegal K character
• Upon detection of link failure, core resets itself and forces link partner to reset
RSBI Transmission

• All data frames have a SOP/SOF and EOP/EOF to indicate the start and end of packet

• User must send at least 2 DWORDs (8 bytes)

• Core will add pad data to allow CRC functionality

• User cannot transmit data in increments less than input width

  — Data can now be transmitted in any increment
RSBI Reception

• Strips off SOP/SOF* and EOP/EOF** from frame
• Strips off pad data if necessary
• Signals any errors detected
• Checks CRC for correctness

*SOP/F = Starting of Packet/Frame
**EOP/F = End of Packet/Frame
Serial Backplane: Full Mesh

Design Approach Supporting
16 slot, 3.125 Gbps per link
Full Mesh Serial Backplane

- 2VP50
- X 15
- RSBI layer
- Rocket I/O Transceivers
Implementing RSBI in Virtex-II Pro Platform FPGA

Implementation in Virtex-II Pro FPGA

- **Features**
  - Up to 40 Gbps
  - 32-bit user interface
  - Low overhead

- **Utilization**
  - 350 Slices
Serial Backplane: Private Connection

Parallel Connection on line card

4 Transceivers Channel Bonded for “Private” board to board connection
Sample Serial Backplane Approaches

- XAUI Switch
- XAUI Core
- Rocket I/O Transceivers
- Backplane
- 2VP20
Implementing XAUI in Virtex-II Pro FPGA

- Implementation in V-II Pro
- Uses 4 Rocket I/O Transceivers
  - Channel bonding
  - 8B/10B encoding
- Utilization
  - 800 Slices
Signal Integrity Design Resources

http://www.xilinx.com/signalintegrity
Figure 4-5: Power Filtering Network for One Transceiver
## Power Filtering Network Components

### Capacitors
- \( C = 0.22\, \text{uF} \)
- Package: 0603 SMT
- Dielectric: X7R
- Tolerance: 10%
- WVDC: 10V
- Spacing: Within 1cm of pin

### Ferrite Beads
- Murata BLM11A102S

### Voltage Regulator
- Linear Technology LT1963

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All parts specified in PCB Design Requirements

Voltage Regulator must use circuit specified by manufacturer
VTTX, VTRX

Top of board

Ferrite Bead

Capacitors
Reference Clock

• Must use EPSON EG-2121CA
  – 2.5V LVPECL output oscillator
  – Use according to manufacture specifications

• Resistor network for clock input:

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<thead>
<tr>
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<tbody>
<tr>
<td>R1</td>
<td>510 ohm</td>
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<tr>
<td>R2</td>
<td>130 ohm</td>
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</tr>
<tr>
<td>R3</td>
<td>25 ohm</td>
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</tr>
<tr>
<td>R4</td>
<td>100 ohm</td>
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Implementation Resources

- Physical (PCB) Design Information
  - Signal Integrity Central on Xilinx Web Site (http://www.xilinx.com/signalintegrity)
  - Rocket I/O User Guide
  - Spice Suite

- RSBI Design Information (http://www.xilinx.com/rsbi)
  - Specification, Implementation notes
  - Source code (Verilog)
  - Test bench

- XAUI information (http://www.xilinx.com/connectivity)
  - In Networking/Datapath Products (10 Gigabit Ethernet)