

Features

- H.264/MPEG-4 Part 10 Main/High/High Ext. Profiles Level 4.2+
- Support for up to HD 1080i and 1080p/60 fps at 75 Mbps.
- Output stream is compliant with International Standard ISO/IEC 14496-10:2005 (E) Rec. H.264 (E)
- Frame or Field processing
- 4:2:0 supported.
- Fixed context model initialization supported
- Interlaced streams supported
- Output stream granularity at single slice level.
- Output control signals provided for rate control and rate distortion optimization
- Self-sustaining internal state machine supported for user interface

Resource Summary

LogiCORE™ Facts Core Specifics		
Supported Device Families	Virtex™-5, Virtex-4, Spartan™-3	
Resources Used		
Virtex-5	1080i/p	5083 Slice Flip Flops 10258 Slice LUTS 8 RAMB18x2, 20 RAMB36
	720i/p	5083 Slice Flip Flops 10258 Slice LUTS 8 RAMB18x2, 20 RAMB36
	ITU-R-BT.601	5072 Slice Flip Flops 10270 Slice LUTS 8 RAMB18x2, 16 RAMB36
	CIF	5022 Slice Flip Flops 10240 Slice LUTS 8 RAMB18x2, 14 RAMB36

LogiCORE™ Facts Core Specifics		
Resources Used		
Virtex-4	1080i/p	49 block RAMs, 8860 slices
	720i/p	49 block RAMs, 8860 slices
	ITU-R-BT.601	41 block RAMs, 8727 slices
	CIF	37 block RAMs, 8627 slices
Spartan-3	ITU-R-BT.601	43 block RAMs, 7942 slices
	CIF	39 block RAMs, 7831 slices
Provided with Core		
Documentation	Data Sheet, User Guide	
Design File Formats	VHDL, EDIF	
Verification	JM10 Reference C-Code vs. VHDL Test Bench and HW Tests	
Instantiation Template	VHDL Wrapper	
Design Tool Requirements		
Synthesis	Synplicity Synplify_Pro 8.6.2	
Xilinx Implementation Tools	Xilinx ISE™ 8.2.03i (from ngd_build)	
Verification	ModelSim® 6.1c SE, MicroSoft Visual C++ V6.0, ActivePerl 5.8.3. Annapolis Micro Systems WildCard4 platform API 3.0, Driver 4.0, Firmware 1.0	
Simulation	ModelSim 6.1c SE	
Support		
Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing functionality, or support of product if implemented in devices not listed in the documentation, or if customized beyond that allowed in the product documentation, or if any changes are made in sections of the design marked DO NOT MODIFY.		

Introduction

The Xilinx H.264 Context Adaptive Binary Arithmetic Coder (CABAC) Version 1.0 core is a fully functional VHDL design implemented on a Xilinx FPGA. For each slice to encode, the CABAC core generates a compressed bitstream as specified by the ITU-T Video Coding Experts Group (VCEG) together with the ISO/IEC Moving Picture Experts Group (MPEG) as the product of a collective partnership effort known as the Joint Video Team (JVT). The collaborative effort is also known as H.264/AVC/MPEG4 Part 10.

A high-level block diagram of the CABAC core is shown in **Figure 1**. The two main components are the control state machines (Main SM and Pre-Processing SM) and the encoding engine. As shown in **Figure 1**, the CABAC core is fully self-sustained with its complex state machines able to effectively generate and feed the appropriate Synthax Element (SE) into its internal Arithmetic Coding (AC) engine. For a given slice (pre-defined partition of a frame), the necessary input data is fed on a macroblock (MB) basis and consists mainly of the integer transform coefficients' absolute levels, the motion vector differences (MVD) and other related information such as MB type and MB prediction mode. The length and size of the MB data given as input to the core is adaptively determined on both the user's side and inside the core itself.

For instance, in the case of an MB that does not contain any MVDs, the core has prior knowledge of this and does not waste cycles waiting for MVDs. Correspondingly, the user does not send any MVDs. Another example is with the transform coefficients of a given MB, which are skipped by both the core and the user's sides when the coded block pattern value is zero. This adaptiveness translates into significant savings of MB data transfer bandwidth between the user's side and the core. The generated SEs are passed to the AC engine block which consists of the AC encoder, the binarizer, and the context management block. After binarization of the input SE, each resulting bit (or bin) is sequentially processed by the encoding engine in a single clock cycle. The ability to process each bin in a single clock cycle coupled with the fast state machines enables real-time HD encoding.

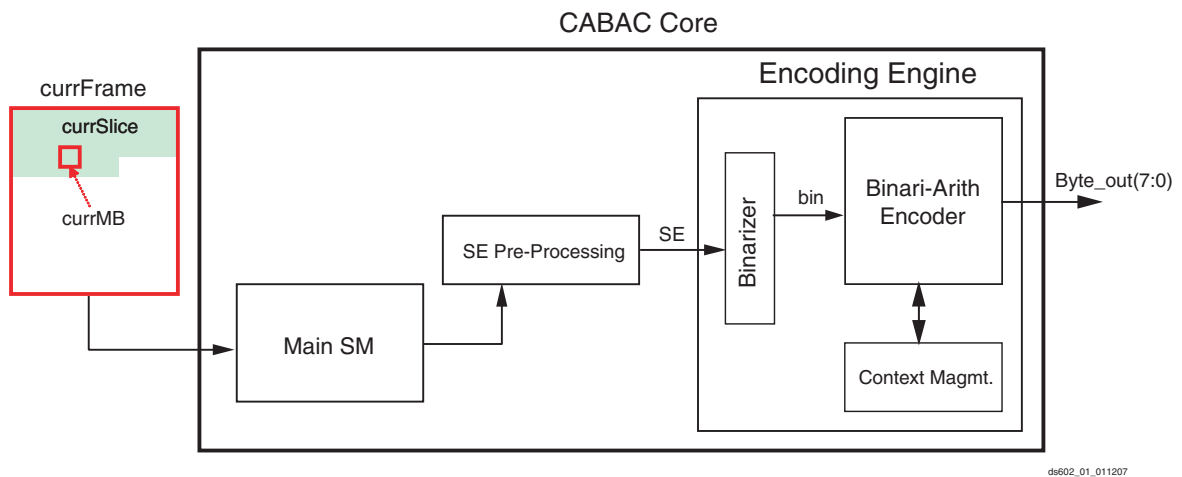


Figure 1: CABAC Functional Block Diagram

Applications

The CABAC Encoder core can be utilized in H.264 standards applications where hardware acceleration is needed to achieve real time operation. Typical video applications are video surveillance, video conferencing, and video broadcast. The CABAC core can also be used in military and medical applications in a standalone application where lossless arithmetic coding is desired.

Performance

Table 1 shows the performance of the CABAC core for different device families and the corresponding output data rate supported.

Table 1: Performance Summary

FPGA Family	Clock FMax	Approximate 4:2:0 Output Bit Rate (Mbps)	Notes
Spartan-3E	50 MHz	25	Supports up to SD, 601i, 4CIF
Virtex-4	133 MHz	66	Supports up to HD, 1080P/30, 1080i/60, 720P/60
Virtex-5	165 MHz	80	Supports up to 1080P/60, 1080i/60, 720P/60

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/15/07	1.0	Initial Xilinx release.