Revolutionary Architecture for the Next Generation Platform FPGAs

Embargoed News:
December 8, 2003
The Evolution of FPGA Architectures

1985: FPGA for glue logic

1987: FPGA for core functionality

1992: FPGA w. soft system IP

2001: Logic Platform w. hard & soft system IP

2002: System Platform w. Processor IP

2004: Domain-specific Platforms

FPGA for core functionality

FPGA w. soft system IP

Logic Platform w. hard & soft system IP

System Platform w. Processor IP

Domain-specific Platforms

FPGA Solution

Meta Architecture
The ASMBL\(^{(TM)}\) Architecture

Application Specific Modular Block Architecture

Column Based ASMBL Architecture

Feature Options
- Logic
- DSP
- Memory
- Processing
- High-speed I/O
- Hard IP
- Mixed Signal
- Future...

Domain A

Domain B

Domain C

Future

Applications
Addressing Geometric Constraints

- I/O and array dependency
- Power & ground distribution
- Hard IP scaling
ASMBL Addresses

I/O and Array Dependency

Array increase, I/O increase

Array constant
I/O increase

Array increase, I/O constant

Peripheral I/O
dependent on array size

Column based I/O
independent of array size
ASMBL Addresses
PWR & GND Distribution

• New Pwr & Gnd distribution reduces voltage drop
• Switching reliability increase via higher thresholds

Traditional Architecture

ASMBL Architecture
ASMBL Addresses
Hard IP Scaling

Array size increase to accommodate feature scaling

Array size constant as features scale independently

Traditional Architecture

ASMBL Architecture
ASML: Advantages

- Xilinx Benefits
  - Reduces time & risk for FPGA platform development
  - Enables cost-effective assembly of multiple platforms
  - Allows rapid response to new market demands

- Customer Benefits
  - Highest value solution at a given price point
  - Right feature mix for a given domain
ASMBL Enables
Domain-Specific Platforms

Right feature mix at the lowest cost
Cost Effectively Expanding Xilinx FPGA Application Domains

Next Gen Virtex Domain A

Virtex-II Pro

Virtex-II

Virtex-E

Virtex

Next Gen Virtex Domain B

Next Gen Virtex Domain D

Next Gen Virtex Domain C

Expand beyond traditional $5.1B PLD Market

Market Data Source: Gartner Dataquest 2007 Projection FPGA/CPLD Market
Taking Advantage of Moore’s Law

Transistor count increases, cost decreases
Taking Advantage of 10+ Layers of Metal

Metal Layers

10+
10
9
8
7
6
5
4
3
2
1


Virtex
Virtex-E
Virtex-II
Virtex-II Pro
Next Gen Virtex

ASMBL Granularity
IP Immersion
Substrate
Taking Advantage of Advanced Packaging

- Flip Chip enables column based architecture
- Allows connecting to I/Os anywhere on the die
- Enhanced thermal dissipation

Package source: Amkor Technology
Next Generation Cost Metrics

Old density based metrics
$/LC and $/Gate

New capability based metrics
$/MAC/s or $/BOPS
$/Mbit of storage
$/Gbps bandwidth
$/Gbyte/s bandwidth
$/DMIPS
$/system functionality
$/mixed signal

Cost per Function

1998 1999 2000 2001 2002 2003 2004 2005
Conclusion

- ASMBL enables domain-specific Platform FPGAs
- Addresses traditional architectural limitations
- Highest value solution at a given price point