

Virtex-II EasyPath FAQs

What is the Virtex-II EasyPath Solution?

Virtex-II EasyPath devices are FPGAs that have been custom tested for a specific customer application. By combining the programmable nature of the FPGA with Xilinx advanced testing methodologies, the fitness of a specific piece of silicon can be guaranteed for a given application. The increased yield associated with the custom testing allows Xilinx to offer these devices at a significantly reduced cost compared to a standard FPGA. Because the Virtex-II EasyPath device implements the specific application in the exact same circuit as an FPGA device, a 100% match to the performance and functionality of the standard FPGA is guaranteed.

When would I use the Virtex-II EasyPath solution?

Sometimes customers design systems using standard FPGAs in the prototyping phase and look for a cost-reduction path for when the system goes into volume production. One approach that some customers take is converting the FPGA to an ASIC. This approach entails significant design risk, requires involved engineering resources, and can take several months to complete. Virtex-II EasyPath solutions give designers comparable cost reduction to custom silicon with none of the risk, engineering resource requirements, or months of development time.

Is it a new product line?

The Virtex-II EasyPath solution is a new product offering from Xilinx. Xilinx is currently offering Virtex-II EasyPath devices for qualifying high-volume applications implemented in several high-density Virtex-II devices, specifically the XC2V3000; XC2V4000; XC2V6000 and XC2V8000. Virtex-II EasyPath solutions are planned for the Virtex-II PRO Platform FPGA family and future high-density FPGA families.

What cost savings can I expect from Virtex-II EasyPath devices?

Depending on density and volume, customers can expect a 30-80% cost reduction when compared to the equivalent standard FPGA.

When will this solution be available?

This solution is available today for the four largest devices in the Virtex-II family. Future devices are currently being planned.

Is there a custom charge?

Yes. The custom charge allows Xilinx to create and validate the coverage of a design specific test program as well as set up the operational processes required for each unique customer requirement. The engineering required for Virtex-II EasyPath devices is most comparable to that of gate array technology that includes automatic test vector (ATV) generation and guarantees a high percentage of test coverage. For equivalent densities, the custom charge for Virtex-II

EasyPath solutions and gate arrays with ATV are priced similarly, but Virtex-II EasyPath devices provide 100% guaranteed test coverage with much lower risk, lead time, and no customer engineering resources required.

For what FPGAs is the Virtex-II EasyPath solution available?

The Virtex-II EasyPath solution is being introduced for the highest density members of the Virtex-II FPGA family: XC2V3000; XC2V4000; XC2V6000 and XC2V8000. Since this solution is primarily software and test driven, support for new FPGAs families can be quickly developed.

What is the difference between Virtex-II EasyPath devices and the Xilinx cost-optimized Spartan-III FPGA family?

Spartan-III FPGAs and Virtex-II EasyPath devices are complimentary solutions that together provide total cost management for a wide spectrum of applications in both medium and high densities. Spartan-III FPGAs offer a performance level and feature set targeted for consumer digital convergence applications while Virtex-II EasyPath solutions offer high-end performance and features identical to the Virtex-II family of FPGAs.

How does the Virtex-II EasyPath solution compare on cost to ASICs?

Overall, Virtex-II EasyPath will offer lower overall costs compared to an ASIC. ASICs may offer lower production unit prices but carry other significant direct and indirect costs. ASIC conversion involves weeks or months of customer engineering time to provide the data for an ASIC manufacturer and to re-verify the solution in system. ASIC conversions have a high risk of delay or failure, which increases upfront costs and delay the lower cost system's release to the market. In addition, an ASIC conversion often cannot match the timing, performance, features, and/or pinout of the original FPGA. The amount of change that is introduced when a netlist is converted from an FPGA architecture to that of a gate array is substantial. The longer the delay in an ASIC conversion, the higher the chance that a customer will either miss a market window or have to continue to ship product with the higher-cost standard FPGA. Virtex-II EasyPath solutions require no customer engineering resources for redesign, test vector generation, re-verification, or re-qualification. They are performance, feature, pin, and package compatible with the original FPGA. In addition, they offer much shorter lead times than an ASIC, meaning you can get your cost reduced product to market much faster than with custom silicon.

Xilinx has developed a comprehensive tool, WebACE, for comparing FPGAs, Virtex-II EasyPath devices, and ASICs. This tool is available at <http://www.xilinx.com/products/webace/>.

What's the turnaround time for a Virtex-II EasyPath order?

Because no custom silicon needs to be processed, Xilinx can offer the best turnaround time of any FPGA cost reduction approach. At the initial order, production volumes can be shipped within 8 weeks. Subsequent orders for the same application can be shipped within a few weeks. With traditional conversion approaches, delays associated with prototype wafer processing,

prototype acceptance/debug, device qualification, system verification testing, and production wafer processing can make lead times several months best case, but can easily extend beyond a year if everything does not go perfectly.

Explain the Virtex-II EasyPath testing technology.

Virtex-II EasyPath devices are standard FPGA circuits that are verified to meet the requirements of a specific customer application. Xilinx has created an innovative test methodology that leverages the re-programmability of FPGAs to isolate and test all resources required by a specific design. Virtex II EasyPath utilizes the same silicon circuit as the Virtex-II. It utilizes a proprietary customer specific test program to assure all interconnects and resources required by the customer design are completely and fully tested including RAM, logic, routing, and circuit operation at speed.

This customer specific testing is done using the same techniques and thoroughness as that used for the FPGA. The exact same tests are used for the “common” with FPGA resources (all the I/Os, configuration circuits, clock trees, etc.) while a customized test program tests all design specific resources. All the necessary information to define a design for use in a Virtex-II EasyPath solution is generated by Xilinx implementation tools. Xilinx then creates a set of configuration patterns and test vectors that are combined into a custom test program. This custom test program validates that all resources required by a specific design are defect free and that any defects that may be present in unused parts of the chip will not affect performance or reliability of the specific application. The result is an application specific device that functions and performs identically to the standard FPGA it replaces.

How do you guarantee that the Virtex-II EasyPath device is both timing and functional compliant with the standard FPGA?

Virtex-II EasyPath devices use exactly the same FPGA design. Typically an FPGA is tested and validated to support ***all possible applications*** while a Virtex-II EasyPath device is tested and guaranteed to meet the needs of a ***specific application***. Since a specific application will be implemented identically in an FPGA or Virtex-II EasyPath device, the performance and operation of the Virtex-II EasyPath device is identical to that of the standard FPGA for that application.

How do you guarantee that the Virtex-II EasyPath device is fully functional with the customer design?

Each Virtex-II EasyPath device is tested to isolate and validate all the resources required by the specific design. The portion of the integrated circuit used is identical whether implemented in an FPGA or a Virtex-II EasyPath device. Xilinx has conducted quality and reliability testing to guarantee the operating life of the Virtex-II EasyPath device. Reliability data can be obtained from Xilinx.

Is there any risk that you would not have enough devices to support a specific application?

Xilinx has developed a detailed understanding of the yield characteristics for Virtex-II EasyPath devices and has determined that yield is nearly independent of the specific application. Supporting large orders for Virtex-II EasyPath devices is no different than large orders for FPGAs. With an understanding of the customer volume requirements, Xilinx is able to manage its supply chain to meet the requirements.

Is this a response to Altera's HardCopy?

Altera's HardCopy is much more like Xilinx's HardWire product introduced in 1995. With the introduction of the Virtex architecture, the complexity of high-density FPGAs made conversion approaches like Xilinx's HardWire and Altera's HardCopy infeasible. Xilinx's Virtex-II EasyPath devices utilize a standard FPGA with custom testing resulting in the first no risk cost reduction vehicle for high-density FPGA devices. The Virtex-II EasyPath solution is a response to the market need for both the fastest time to market as well as lowest total cost.

How is this different from HardWire?

Virtex-II EasyPath devices differ fundamentally from HardWire in that no custom silicon is utilized. Virtex-II EasyPath devices offer a cost reduction from FPGA designs through advanced test methods that guarantee fitness for a specific design. The result is a 100% match to the same circuit running in an FPGA. HardWire devices are manufactured using a design conversion process that retargets programmable logic devices to a more cost efficient fixed implementation.

Why did we drop the HardWire business?

With the introduction of the high-performance Virtex architecture, Xilinx realized that a design conversion approach to a HardWire technology was no longer feasible. Virtex advanced features such as block RAM, clock management and flexible, high speed blocks are already optimized within the standard FPGA. Reducing silicon area would be feasible by replacing programmable interconnect with fixed interconnect, but the timing relationships among interconnect paths cannot be consistently maintained. As technology continues to shrink, the routing becomes a larger component of the delay increasing the difficulty of matching the FPGA timing by using a custom design conversion. Xilinx concluded converting deep sub-micron FPGA devices using Hardwire offered neither time to market advantages nor could a high success rate be guaranteed due to these timing differences.

What stops competitors from delivering an equivalent product?

Xilinx has spent significant time and resources developing this cost-reduction approach. It would be a non-trivial investment of time and money for a competitor to offer a similar solution. In addition, Xilinx is working to put protections in place for the intellectual property for testing and other aspects behind this approach.