

## 6.1i Partner Tool Device Matrix

Xilinx Device Family	Virtex-E	Virtex-II	Virtex-II Pro	Spartan-II	Spartan-IIe	Spartan-3	CoolRunner-II
<b>Partner Tools</b>							
<b>HDL Linters</b>							
Synopsys LEDA 3.3	X	X	X	X	X	X	
Atrenta SpyGlass 3.1		X	X				
<b>HDL Synthesis</b>							
Synplicity Synplify (Pro) 7.3.1	X	X	X	X	X	X	X
Mentor LeonardoSpectrum 2003b	X	X	X	X	X	X	X
Mentor Precision RTL Synthesis 2003b	X	X	X	X	X	X	X
Synopsys FPGA Compiler II 3.7.2	X	X	X	X	X	X	
Synopsys Design Compiler 2003.06	X	X	X	X	X	X	
<b>Physical Optimization</b>							
Synplicity Amplify 3.2.3	X	X	X	X	X		
Magma/Aplus Design PALACE	X	X	X	X	X		
<b>RTL Debugger</b>							
Synplicity Identify 1.2	X	X	X	X	X		
<b>ASIC Prototyping</b>							
Synplicity Certify 6.2.3	X	X	X				
<b>Co-Design</b>							
Celoxica DK-1 1.1	X	X	X	X	X		
CoWare N2C 3.2			X				
Endeavor Co-Simple 2.4			X				
Mentor Seamless 4.3			X				
Novilit Protocol AnyWare 2.1		X	X				
<b>Schematic Entry/Gate Level Simulation</b>							
Innoveda ePD - Fusion 3.0	X	X	X	X	X		X
Mentor Design Architect - Quicksim version D.1	X	X		X	X		
Cadence Concept 14.2	X	X		X	X		X
<b>HDL Simulation</b>							
Mentor ModelSim 5.7b (VHDL/Verilog)	X	X	X	X	X	X	X
Cadence Verilog-XL 5.0	X	X	Solaris-only	X	X	X	X
Cadence NC-Sim (VHDL/Verilog) 5.0	X	X	X	X	X	X	X
Synopsys VCS_MX7.0.1	X	X	Linux & Solaris only	X	X	X	X
Synopsys Scirocco 2002.12	Contact Factory for VHDL design support						
<b>Formal Verification</b>							
Synopsys Formality 2003.9	X	X	X	X	X	X	
Verplex - Conformal-FPGA 4.1	X	X	X	X	X	X	
<b>Chip Level Static Timing</b>							
Synopsys PrimeTime 2003.09		X	X			X	
<b>Board Level Static Timing</b>							
Mentor Tau 3.1	X	X	X	X	X	X	X
<b>Board Level Signal Integrity</b>							
Mentor Hyperlynx 7.0	X	X	X	X	X		X
Mentor ICX 3.1	X	X	X	X	X		X
Cadence SPECCTRAQuest 15.0	X	X	X	X	X		X
Synopsys HSPICE 2003.9			X				
<b>Embedded Tools and RTOS</b>							
Windows VxWorks 5.5			X				
Mentor Nucleus PLUS 1.14.1 (MicroBlaze)	X	X	X	X	X	X	
Monta Vista Professional Edition v3.0			X				