

Virtex-II Pro Platform FPGA Family

Product Backgrounder

The Virtex®-II Pro Platform FPGA solution is arguably the most technically sophisticated silicon and software product in the programmable logic industry. The goal in developing the Virtex-II Pro FPGA was to revolutionize system architecture “from the ground up.” To achieve that objective, circuit engineers and system architects from IBM, Mindspeed, and Xilinx co-developed this advanced Platform FPGA. Engineering teams from top embedded systems companies, including Wind River Systems and Celoxica, worked together with Xilinx® software teams to develop the systems software and IP solutions that enable new system architecture. The result is the first Platform FPGA solution capable of implementing ultra-high bandwidth SoC (system-on-a-chip) designs that were previously the exclusive domain of custom ASICs, yet with the flexibility and low development cost of programmable logic. This new solution is expected to usher a new era of leading-edge system architectures in networking applications, embedded systems, and digital signal processing systems.

Virtex-II Pro Family Features

- Five family members with 3,168 to 50,832 logic cells and 216 to 3,888 Kbits of Block RAM
- Based upon Virtex-II IP-Immersion architecture
- Multi-gigabit (3.125 Gb/s) serial transceiver blocks, up to 16 per device
- PowerPC embedded processor cores, up to four per device

Virtex-II Pro Family Key Value Proposition

- Platform for Programmable Systems
- Enables architectural synthesis
- Delivers next generation connectivity standards
- Enables a new development paradigm
- Delivers leading edge price/performance value

Virtex-II Pro Family Highlights

The Virtex-II Pro family consists of five members, each with four to 16 RocketIO™ multi-gigabit transceivers based on the Mindspeed SkyRail™ technology. Unlike the basic clock/data recovery block provided in the first generation of embedded programmable products, each Xilinx RocketIO block contains a complete set of user-configurable support circuitry that addresses real-life system-level challenges. This circuitry includes standard 8B/10B encode/decode, support for higher bandwidth using multiple channels, and support for improved signal integrity across varying PCB trace lengths. In addition, the RocketIO blocks are the first FPGA-embedded transceivers to reach a baud rate of 3.125 Gb/s. Four RocketIO blocks allow 16 PCB traces to support full-duplex 10 Gb/s data rates. This is equivalent to 256 traces of typical busses or 68 traces of a high-speed parallel bus. This allows a PCB trace reduction of up to 16X over conventional parallel busses, resulting in significant reduction of PCB complexity and EMI system noise. The RocketIO technology allows higher bandwidth system than currently possible, with cost savings from faster time-to-market, reduced printed circuit board (PCB) size, and lower component count.

Virtex-II Pro Technical Backgrounder

The Virtex-II Pro members also incorporate small yet powerful PowerPC processor cores. Each of the larger Virtex-II Pro devices incorporates one to four IBM PowerPC 405 processor cores, each capable of more than 300 MHz clock frequency and 420 Dhrystone MIPS. While the PowerPC 405 core occupies a small portion of the die area, it provides tremendous system flexibility. The PowerPC 405 cores are fully embedded within the FPGA fabric, where all processor nodes are connected by the FPGA routing resources. This provides the utmost architectural capability, where complex applications may be efficiently divided between high-speed implementation in logic and high-flexibility implementation in software. For example, a packet processing application using only the FPGA logic today for high-speed packet routing may be augmented to include a slave high-performance processor for exception handling or in-system statistics monitoring. In contrast, using a separate processor externally in these applications would require additional interface pins, which degrades the system performance, and significantly increases FPGA I/O requirements and overall board costs.

The Virtex-II Pro products are built on the popular Virtex-II architecture with IP-Immersion technology. Unique features common in the Virtex-II series – comprising Virtex-II and Virtex-II Pro families– include SystemIO™ connectivity solutions, XCITE™ digitally controlled impedance technology, comprehensive clocking solutions, high-speed Active Interconnect routing architecture, and bit-stream encryption. All these features together comprise the complete Platform FPGA solutions optimized for high-performance system-level applications to deliver faster time-to-market, engineering productivity, and system flexibility.

Continuing Legacy of Virtex Technology Leadership

- Both serial transceivers and embedded processor cores
- 0.13 micron 9-layer copper low-k process technology
- 3.125 Gb/s embedded multi-gigabit transceivers
- 300+ MHz, 420 D-MIPS PowerPC processor cores

Each of the Virtex families of FPGAs has been successful programmable product family in its class, starting with the introduction of the original Virtex family in 1998. The Virtex and Virtex-E families have been hailed by the industry as technologically advanced products when they were first introduced. The Virtex-II family, which again achieves technology leadership in density, performance, and features, was the first example of Platform FPGAs – programmable devices with the features and performance to implement systems functionality.

The Virtex-II Pro family is the first FPGA family to incorporate *both serial transceiver technology and a hard processor core* within a general-purpose FPGA device. This is significant for new high-bandwidth embedded processing applications such as packet processing, where both high I/O bandwidth and high-performance processor cores are needed together.

The Virtex-II Pro devices use the *advanced 0.13-micron 9-layer copper* process. This IBM all-copper low-k technology is the most advanced production process in the semiconductor industry. The combination of this process technology and the Active Interconnect architecture delivers higher performance than any FPGA.

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The RocketIO multi-gigabit transceivers based on Mindspeed SkyRail™ technology, are *high performance* and *complete* CMOS embedded serial transceivers. They are user-configurable for up to 3.125 Gb/s baud rate per channel, which is over twice the performance of other embedded transceivers at 1.25 Gb/s. Each RocketIO block provides a complete set of common functionality available in standard SerDes transceivers including both the Physical Coding Sub-layer (PCS) and the Physical Media Attachment (PMA). In contrast, “programmable ASSP” products with clock/data recovery (CDR) provide only the most basic transceiver capability.

The IBM PowerPC 405 processor core used in the Virtex-II Pro family is the *highest performance* embedded processor available in any FPGA. The PowerPC architecture is used in many markets including communications, industrial control, as well as test and measurement systems.

Complete RocketIO SerDes Capability

- Four to 16 channels of multi-gigabit transceivers
- 622 Mb/s to 3.125 Gb/s data rates per channel
- Built-in optional 8B/10B, pre-emphasis, channel bonding capabilities

Virtex-II Pro devices have from four to 16 RocketIO blocks. Each RocketIO block supports a baud rate of 622 Mb/s up to 3.125 Gb/s per full-duplex channel, using the proven Mindspeed SkyRail technology. RocketIO blocks incorporate built-in user-configurable support for 8B/10B encode/decode, output pre-emphasis, channel bonding, and comma detect. The RocketIO blocks are used in conjunction with SystemIO soft IP cores to support emerging interface standards and protocols such as XAUI (for 10 Gigabit Ethernet) and Gigabit Ethernet.

RocketIO blocks provide significant benefits over conventional parallel I/O standards for high-bandwidth data transfer. For example, 256 PCB traces are needed to implement a full-duplex (i.e. both transmit and receive) 10 gigabit per second interface using two 128-bit wide synchronous LVTTTL busses at 78 MHz. The same data bandwidth may be implemented using only 16 PCB traces—94 percent less PCB routing area—by using four RocketIO blocks. Compared to wide parallel busses, the high-speed serial interface uses less board area with less power dissipation.

Example 10 Gb/s interface

In a typical advance application, the XC2VP4™ Virtex-II Pro device is used to implement a full-duplex 10 Gb/s back-plane interface to another board containing a Mindspeed quad SerDes. Such an interface requires four RocketIO blocks and 16 back-plane traces. Because the Virtex-II Pro device is compatible with the Mindspeed SkyRail device, the 4 serial output pairs and 4 serial input pairs in the XC2VP4 may be connected directly to the corresponding 4 input and output pairs, respectively. Each 10 Gb/s of output data is driven by 128-bit wide internal busses that are fed into four RocketIO blocks, which are separately serialized and encoded using the same clock. In this case, there are 32 bits of data at 78 MHz driving a RocketIO block. Each 8-bit byte of the 32-bit data is encoded into a 10-bit code using the 8B/10B encoding standard, whereby the output data stream is encoded to have closely spaced transitions, as well as an equal number of 0's and 1's on average. The former ensures that there are sufficient edges to allow the clock to be recovered accurately, even when the received data consists of unlimited strings of 0's or 1's. The latter ensures that the output differential pair is “DC balanced,” with a stable average voltage,

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independent of the data-stream. Using 8B/10B, the output operates at 3.125 Gb/s baud rate ($= 10/8 * 32 * 78 \text{ MHz}$), with a data rate of 2.5 Gb/s ($= 32 * 78 \text{ MHz}$).

The four differential signal pairs may be routed from the outer pins of the XC2VP4 package to the Mindspeed quad SerDes through a high-frequency edge connector, the back-plane, and another high-frequency edge connector. Along the way, high-speed PCB layout techniques must be used to ensure that stringent signal integrity requirements are met, and the signal path must be fully simulated. The RocketIO blocks are designed to drive up to 24 inches of FR-4 PCB material, by providing four levels of programmable signal pre-emphasis. For example, short signal traces experience minimal attenuation, so only the default 10 percent pre-emphasis is needed. Longer signal traces will cause high frequency signal attenuation, which results in a gradual closing of the differential signal window (called the “eye”). In that case, pre-emphasis may be added at the output driver via device configuration, whereby the output driver momentarily over-drives each new data bit, in order to compensate for signal attenuation. The result is wider differential separation at the receive side, thus better data integrity.

On the receive side, the four differential channels must be deserialized individually, and then re-synchronized together to a common clock in order to reconstruct the 128-bit transmit data. Within the Virtex-II Pro device on the receive side, each RocketIO block deserializes the incoming encoded data-stream by extracting both the clock and data signals. Clock information is inferred by the data transitions using 8B/10B encoding. The extracted clock is used to register the incoming data, which is decoded back from the 10-bit codes into 8-bit data.

The four serial channels are channel-bonded to form a single 10 Gb/s data-rate pipe rather than four separate 2.5 Gb/s data-rate pipes. Therefore, three of the receiving RocketIO blocks must re-synchronize their data to the extracted clock of the fourth designated master RocketIO block. This is necessary because there may be small differences in propagation delay among the four channels due to slight differences in trace lengths, causing the four recovered clocks to differ. Each RocketIO block contains an elastic buffer to re-align the channels relative to the master clock. The alignment is determined by the automatic training sequences that are sent before any data transmissions commence.

There is also a need for control characters to be sent from the transmitters to the receivers for such commands as starting training sequences, request re-transmissions, or flushing buffers. These special commands, called “comma” characters, use special codes that do not correspond to any data words. Automatic comma detection is built into each RocketIO block.

In summary, the RocketIO blocks offer superior functionality and user programmability with built-in 8B/10B, channel bonding, signal pre-emphasis, and comma detect. The RocketIO blocks work with the soft IP library of the SystemIO solution to provide fast pre-engineered connectivity solutions in advance systems.

Powerful PowerPC Embedded Processor Core

- One to four embedded PowerPC 405 cores
- 420+ Dhrystone MIPS at 300+ MHz clock frequency
- Powerful OCM™ controllers allow new architecture paradigms

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- 64-bit CoreConnect™ soft bus

The PowerPC 405 core is an embedded processor core with a 32-bit Harvard architecture optimized for high performance, small die area, and low power. The PowerPC core incorporated in the Virtex-II Pro FPGA is a 0.13 micron implementation of the proven, area-optimized 0.18 micron IBM PowerPC 405 used in the IBM Blue Logic™ core library. Specialized user-configurable logic interfaces all the nodes of the core to the FPGA fabric, so that the resulting connections are fully programmable within the Xilinx ISE software by the user. In this way, all 700 I/O nodes of the core may be used by the user design to achieve tremendous processing bandwidth. In contrast, a separate processor device with a limited bus interface to FPGA fabric cannot achieve this level of bandwidth due to I/O pin limitations. Each of the larger Virtex-II Pro devices has one, two, or four embedded PowerPC 405 processors.

The PowerPC 405 core runs at over 300 MHz clock frequency with an estimated rating of over 420 Dhrystone MIPS. It incorporates a complete set of functionality, including separate 16 Kbyte instruction and data caches, memory management unit, along with timers and debug circuitry. The result is an SoC processor core tightly coupled with the programmable flexibility of Platform FPGAs.

The PowerPC 405 core has unique On-Chip Memory (OCM) controllers that can provide fast access to a fixed amount of instruction and data memory without using the processor bus. The dual-port Block RAM within the Virtex-II Pro architecture may be used for the separate Instruction-Side and Data-Side OCM. The ISOCM and DSOCM can address up to 128 Kbytes and 64 Kbytes, respectively, depending on the number of Block RAMs available. This capability allows very high system bandwidth to be attained in certain classes of applications, such as “intelligent memories” and fast table lookup, as memory transfers are not subject to processor bus latency. The combination of the flexible FPGA fabric and the dual-port OCM capability provides system architecture flexibility previously unattainable in a programmable platform.

The OCM capability allows many embedded applications to run efficiently with either a small processor bus or no processor bus at all. Applications with code space less than 128 Kbytes and data space less than 64 Kbytes may fit entirely within the Virtex-II Pro device. For example, a small packet-processing engine may be implemented using a single PowerPC 405 core with several Block RAMs for high-bandwidth header manipulation. In these cases, the application can be completely implemented within the Platform FPGA without requiring additional device I/O pins or external memory. Many FPGA applications contain complex state machines, data monitoring functions, or exception handling functions that currently require excessive FPGA logic resources or external components. These can now be efficiently implemented using the PowerPC 405 core with its OCM capability saving the logic resources for high-speed data processing.

For traditional embedded processing applications with higher system complexity, the PowerPC 405 core may be used as the central processing unit, or a system co-processor. For example, a single PowerPC 405 processor core may be used to run Wind River Systems' VxWorks or Linux, while other PowerPC 405 cores may be used as communications co-processors or complex state machine engines. In addition to multiple embedded PowerPC processors available in Virtex-II

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Pro devices, Xilinx MicroBlaze™ soft processor cores may also be introduced into the FPGA fabric. In this way, system processing capabilities may be scaled by using as few or as many processors as needed. Because each PowerPC 405 core occupies only a small percentage of the overall die area, the PowerPC 405 offers a low-cost yet powerful tool for new system architectures.

For complex PowerPC 405 applications, the IBM CoreConnect™ bus architecture is available to support high-bandwidth 64-bit bus at 100 to 133 MHz. The CoreConnect architecture was developed to ease the integration and enable reuse of system and peripheral cores. It comprises the processor local bus (PLB) for high-speed data transfer, on-chip peripheral bus (OPB) for general-purpose, and device control register (DCR) bus for system control. For maximum flexibility, the CoreConnect architecture is implemented within the Virtex-II Pro FPGA fabric. Users can select CoreConnect peripheral IP from an extensive library or develop their own CoreConnect peripherals. For example, a custom communications processor may be developed by using any combination of SDRAM controllers, PCI interfaces, Gigabit Ethernet MACs, UARTs, or other peripherals from a growing library of soft IP peripherals from Xilinx. Specialized user-defined peripherals such as MPX processor bus bridges, echo-canceling algorithm engines, or soft floating point units may be interfaced to the CoreConnect architecture using a standard bus interface macro. Once the peripheral is completed, it may be easily reused in future applications. The processor peripherals developed for the OPB are also compatible with the MicroBlaze soft processor for additional system flexibility.

Industry leading Embedded Tools

Xilinx is working with Wind River Systems, the market leader in the embedded industry, to provide a robust set of software tools for targeting the PowerPC 405 processor in the Virtex-II Pro FPGAs. Wind River Systems has wide market acceptance with their broad range of development tools, Real Time Operating Systems (RTOS) and middleware solutions. A specific Virtex-II Pro version of the Wind River tools (compiler, software debugger and JTAG run control hardware probe) have been created for Xilinx distribution via an OEM agreement. These include

- Diab™ Compiler
- SingleStep™ with vision, Software Debugger
- visionPROBE II JTAG Run Control Hardware Connection Probe

The *Diab C/C++ Compiler* is optimized for the PowerPC processor and provides fine-grained control of the compiler options. It allows users to balance speed, code size and memory usage for their applications. The front end of the Diab product is a language parser, which creates a language-independent representation and this unleashes the power of the five different back-end optimizer stages of the compiler. Diab provides optimization for global, code selector, code generator, peephole and instruction scheduler stages as well as supporting architecture specific features in the IBM PowerPC 405 processor.

SingleStep with vision is a multi-windowed, full featured embedded software debug tool that is far superior to command line tools. This product is ideally suited for board/hardware bring-up and both driver/firmware development as well as software debugging (thus reducing the

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requirements from two or more possible tools to just one). Software debuggers need to provide basic “run, start, stop” control to debug an embedded system, but SingleStep exceeds these expectations as one of the most feature rich debuggers available.

SingleStep supports real-time target control, high-speed downloads, built-in hardware diagnostics and Flash memory programming. It provides a unique processor specific register interface to enable configuring and initializing integrated peripherals and a command line interface with scripting language to automate testing.

This debugger provides PowerPC 405 processor support through hardware breakpoints and a register window. In addition to On-Chip trace, SingleStep provides visibility for instruction completion, branch taken, exception taken, data address compare, and other power debug events.

The *visionPROBE II* provides a high-speed parallel connection between the SingleStep with vision host debugger and the Virtex-II Pro target device. This product allows JTAG run control of the target for system debugging and executing high speed downloads up to 400 Kbytes/s. The probe facilitates register initialization, hardware diagnostics, Flash programming, and hardware breakpoints.

Xilinx and Wind River Systems have collaborated in a strategic partnership for embedded systems development. The collaboration is expected to lead to further tools integration and new product introductions.

For those with ultra tight tool budgets and minimum tool requirements, Xilinx has created a specific version of the popular GNU compiler/debugger tool chain for the Virtex-II Pro family as well as the MicroBlaze soft processor. This allows Xilinx to provide a low cost software tool chain that can be supported in the public domain rather than by Xilinx customer support. Documentation is available on the web and third party companies can offer consulting services for supporting GNU. These include

- gcc – Compiler (Xilinx Virtex-II Pro specific)
- gdb – Software Debugger (Xilinx Virtex-II Pro specific)
- Xilinx Parallel IV cable - JTAG Run Control Hardware Connection Probe

Real Time Operating System (RTOS)

Depending on the complexity of the user application, an embedded system design may or may not require a hard-real-time operating system. For a hardware engineer experimenting with a gate consuming protocol or algorithm, some simple C/C++ code may be all that is required. For other more complex applications which have tight requirements for fast interrupts, maximum uptime and minimum latency, a robust RTOS may be required. Xilinx supports the WindRiver Systems' VxWorks® RTOS and provides WindRiver Systems certified Xilinx *Board Support Package* (BSP) for reference boards.

Advanced FPGA Fabric

- IP-Immersion™ architecture enables Platform FPGA

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- Fourth generation segmented routing technology optimized for fast, wide busses
- Flexible SelectIO-Ultra™ technology supporting 840 Mb/s IOs, with up to 852 user I/O pins (426 differential I/O pairs, excluding the RocketIO serial I/O pairs)
- Xilinx Controlled Impedance Technology (XCITE) capability, providing built-in impedance matching on all single-ended I/Os for signal integrity
- Embedded 18Kbit dual-port Block RAM resources
- Embedded 18-bit x 18-bit multiplier blocks
- DCM (digital clock manager) hard-macros supporting de-skew and frequency/phase manipulation
- Bit-stream encryption for design protection

The Virtex-II series is a comprehensive Platform FPGA solution for high-performance systems. The feature set, built on the advanced FPGA process technology, provides a tool set for system manufacturers to achieve rapid time-to-market, superior engineering productivity, and lowest cost of development.

Intellectual Property Solutions

The Virtex-II Pro Platform FPGA solution includes a comprehensive library of intellectual property (IP) solutions. The Xilinx IP solution enables designers to address nearly any application using the Virtex-II Pro Platform FPGA. Three key application areas are SystemIO Interface solutions for connectivity, Empower Processing solutions including PowerPC processors and MicroBlaze soft processors, and XtremeDSP solutions for digital signal processing systems.

The Processor System Generator tool enables processor based embedded system design with a growing library of IP for processor peripherals. It can help create a complete embedded system using the processor, peripherals and the CoreConnect bus technology. Peripheral soft IP cores available from Xilinx that are normally part of any embedded system include UARTs, arbiters, general-purpose I/O, timer/counters, memory interfaces, Gigabit Ethernet MAC and others. Connectivity cores support existing and emerging multi-gigabit serial and parallel standards. Some examples include 10 Gigabit Ethernet MAC with XAUI interface, 1 Gigabit Ethernet MAC with Gigabit PHY, RapidIO, POS-PHY, Flexbus, PCI, PCI-X among others. DSP cores include both basic building blocks such as filters and FFTs, as well as more complex functions such as Reed-Solomon encoders and decoders and Viterbi decoders. Xilinx also provides the System Generator tool, developed in partnership with The MathWorks that enables designers to move from the traditional DSP processor world to the FPGA world and harness the performance and flexibility they desire.

All cores are pre-engineered and verified to increase engineering productivity and reduce time-to-market. In addition to the IP itself, the Xilinx solution includes tools, training, boards, reference designs, and partnerships. Additional information is available on the IP Center at www.xilinx.com/ipcenter.

Powerful New System Capabilities

- Low latency network processing
- Protocol bridges for next generation connectivity standards

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- Platform for Architectural Synthesis
- Enables a new development paradigm
- Complex embedded systems

The Virtex-II Pro family provides a programmable system platform for network processing where low latency is required, such as storage area networks, wireless infrastructure, and voice over IP networks. The digital convergence phenomenon drives the need for prioritized packet routing based on type and priority. For example, live voice and video data packets require significantly lower latency than data file packets. New data networking applications must now handle higher bandwidth traffic as well as new service levels and priority. In many cases, Virtex-II Pro devices can offer higher overall performance than other solutions, even specialized network processors (NPs). Using the Virtex-II Pro architecture, the most common packets may be quickly read and routed using the FPGA logic, without incurring lengthy software run-time needed with NPs. The FPGA logic interrupts the PowerPC processor core only when processor instructions are needed for special packet types. For example, packets may be stored into a 16 Kbyte dual-port memory area accessible by both the FPGA logic and the PowerPC 405 OCM port, which allow rapid change of control and packet disposition. By using the FPGA logic to process the frequent cases, and the processor core acting as a slave to the logic for infrequent cases, the Virtex-II Pro architecture can provide higher overall performance than NPs and more sophisticated processing capabilities than just FPGA logic.

The Virtex-II Pro solution is suited as a protocol bridge in order to tie together disparate data streams using the next generation connectivity standards. New serial protocols include Gigabit Ethernet, 10 Gigabit Ethernet XAUI, 3GIO, Serial ATA, Infiniband, and Fibre Channel. These must interface seamlessly with each other and to established parallel standards such as PCI, PCI-X, POS PHY Level 3/4, Flexbus 3/4, RapidIO, and 840 Mb/s LVDS. This presents a significant challenge to system developers because of the changing standards, paucity of off-the-shelf interface components, and inflexibility of available solutions. System designers have had to assemble their own blend of FPGAs, discrete physical transceivers, and discrete communications processors to solve their complex system challenges. Even newer “programmable ASSPs” with built-in serial transceivers fall short, because they frequently require companion FPGAs to supplement their logic capacity. The Virtex-II Pro solution, using the powerful Xilinx SystemIO capability to fully integrate silicon, software, and IP cores, provides the most flexible pre-engineered protocol bridge solutions for fast time-to-market and low development costs.

The Virtex-II Pro solution offers an architectural synthesis platform for complex embedded systems found in signal processing, industrial control, image processing, and aeronautic applications. For the first time, complex embedded systems traditionally involving sophisticated hardware and complex software may be developed concurrently, emulated in actual hardware at speed, debugged in-system, and re-architected for performance within days and weeks, rather than months or years. The Virtex-II Pro architecture provides the rich logic, memory, I/O, and processing resources to allow emerging architectural synthesis tools to enable flexible partitioning of the hardware and software throughout the product life cycle. In many cases, higher density Virtex-II Pro components may be used for early system development, whereby extra resources (including additional PowerPC processor cores) may be used to emulate board-level components yet to be developed. This flexibility, obviously unavailable in custom ASICs

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or ASSPs, allows systems to be “emulated” at speed, rather than simulated using software simulators at 100 or 1000 times slower. Full systems may be remotely upgraded as easily as software-only upgrades are done today, using Compact Flash, CDROM, Internet, wireless transmission, or other flexible means. System design is simplified using development software and a large soft IP library to assemble logic- and processor-based platforms.

The Virtex-II Pro solution enables a new paradigm in system development with hand-in-hand design and debug of hardware and software with significant benefits in engineering productivity. Software development may be started earlier using the real device with pre-configured sample platforms, without waiting for the new system board to be developed. Embedded processors can be used for rapid system pre-production and to allow accelerated software development. A preliminary hardware platform can be built quickly, initially emulated as a C-based algorithm using the embedded processors. In addition, hardware and software debug can be performed with real time observability even while both implementations may continue to be speed-optimized.

With the Xilinx ChipScope Pro tool, users will be able to insert logic analysis and bus analysis cores directly into a design, accessing individual signals and bus transactions. Users will be able to analyze the data from these cores using the ChipScope Pro interfaces that communicate with the cores via the IEEE 1149.1 (JTAG) test access port. ChipScope Pro provides users the ability to capture and display information about CoreConnect bus transactions that occur between the embedded processor and IP components implemented in the FPGA fabric. The visibility of on-chip signal behavior provides an order of magnitude improvement in engineering productivity, only available in Xilinx FPGA logic.

Complex embedded systems can be optimally re-partitioned between FPGA logic and processor cores, which allows a continuum of possible tradeoffs between the speed of logic and the flexibility of software code. For example, a first implementation of an echo cancellation algorithm may be all-software in compiled C code running on a PowerPC core, in order to allow the system software development to start. As the system is further optimized, part of the DSP algorithm may be re-targeted using Xilinx System Generator™ and The MathWorks MATLAB®/Simulink® into FPGA logic to achieve a significantly faster but functionally identical system for production release. In this way, there is tremendous flexibility to allow system designers and architects to optimize the tradeoffs in development time, system performance, and system costs.

It is significant that the embedded systems enabled by Virtex-II Pro solutions are “all-soft,” in that both logic and software code are both controlled by a soft data file. This facilitates a low cost of design maintenance and improves design re-use. Whole system upgrade, including hardware and software, can now be done as one unified soft file using the SystemACE configuration solutions, and can be accomplished with the low-cost and ease-of-use as software-only upgrades are today.

The Virtex-II Pro family enables leadership capabilities while delivering leading edge price/performance value. The high integration of the multi-gigabit transceivers and multiple processor cores reduces component cost, PCB real estate, power consumption, and system development effort.

Advantages Over Alternative Non-Reconfigurable Solutions

- Custom ASICs
- Fixed-function chip sets and ASSPs
- Multi-chip solutions with discrete components

The Virtex-II Series offers significantly faster time-to-market and lower development costs than ASICs. Compared to a full-custom ASIC, the Virtex-II Pro solution eliminates the need for exhaustive verification during development, and allows hardware-software debug at system speed rather than slow software simulations. In addition, the Virtex-II Pro features of XCITE signal integrity, pre-engineered clocking capabilities, and abundance of soft IP cores significantly reduce the time required during various points of the development cycle.

The Virtex-II series offers significantly lower development costs than ASICs, due to lower tool costs, lower third party IP costs, and lack of NRE costs. The Virtex-II series also increases engineering productivity by accelerating hardware availability for software development, and increasing software debug speed. In addition, the availability of powerful development tools enables straightforward re-targeting of ARM- or MIPS-based embedded processors into the PowerPC platform. In most cases, the PowerPC 405 core provides higher performance and more powerful capabilities than common ARM or MIPS processor cores, accelerating pre-production of performance-sensitive applications.

Many high bandwidth systems today use large FPGAs together with discrete SerDes transceivers, discrete communications processors, or other discrete components. The Virtex-II Pro family can incorporate many of these components for shorter time-to-market, better performance, and also system cost benefits. Multi-chip solutions using FPGAs and other devices typically require over a hundred I/O pins to interface to each discrete quad 3.125 Gb/s SerDes transceiver or discrete microprocessor. The result is increased PCB complexity to accommodate hundreds of PCB traces, reduced system performance due to on-chip/off-chip connections, and higher overall system costs. In many cases, reducing the pin-count helps the user to choose the FPGA based on logic density and feature needs instead of available I/O pins thus keeping the overall system costs low. In such cases, the Virtex-II Pro devices can integrate the discrete components to achieve faster system development, higher system performance, and lower costs.

The flexibility inherent in the Virtex-II Pro platform enables Programmable System design allowing system architects to fine-tune their architectural tradeoffs *after* the initial prototype is developed. That is, each sub-system function may be freely implemented as hardware-only, software-only, or any combination within the hardware-software continuum, depending on the tradeoff between performance and complexity. For example, a wireless infrastructure system may initially implement a rake filter function in hardware, and then change to a firmware implementation as more software control is necessary during later development. This would be impossible in custom ASICs without significant time and cost penalties.

The Virtex-II series offers significantly more flexibility than fixed chip sets and ASSPs, allowing end-user product differentiation and predictable future support. For a design that can generally be met in either ASSPs or Virtex-II Platform FPGAs, the initial design investment for an FPGA

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implementation may be higher. However, the advantages for Platform FPGA implementations include the customization of functionality, the ease of design reuse, the ability to fix design bugs, the differentiation of the user end products, and the ownership and control of the entire system. These are important in highly competitive markets where ASSPs have standing errata lists and unpredictable future availability. In contrast, properly developed Platform FPGA designs are soft designs that may be readily maintained and re-used as needed. System manufacturers can use the Virtex-II Pro platform for complete programmable systems with greater competitive advantage in the short term, and greater ownership and control over their products in the long term.