

Xilinx Virtex-II Pro FPGAs Questions and Answers

THE VIRTEX®-II PRO FAMILY:

How is the Virtex-II Pro family a Platform FPGA for programmable systems?

Programmable Systems are a new paradigm to describe leading edge system architectures that encompass the tightly coupled nature of hardware and software in a single platform.

By deeply embedding processor cores within the FPGA fabric, the Virtex-II Pro architecture provides the tight coupling needed between the high performance processing engine and the high-speed programmable logic. Together, the two components enable the optimal yet flexible partitioning of software and hardware of a programmable system.

The Platform FPGA provides a single platform that is easily customizable for a broad range of applications- an initiative announced by Xilinx in November 2000. Platform FPGAs allow seamless diffusion of hard IP and soft IP cores of any size or shape into the fabric at any location using IP-Immersion and Active Interconnect technologies. This facilitates Xilinx to immerse hard IP cores such as serial transceivers, processors, Block RAM, and multipliers into the Platform FPGA fabric and provide a scalable platform with ever-increasing capability. It facilitates customers to integrate soft IP obtained from Xilinx and other vendors. The Virtex-II family was the first Platform FPGA announced by Xilinx in early 2001. The Virtex-II Pro family with the embedded PowerPC® and RocketIO™ cores represents the second generation Platform FPGA.

How will the delivery of an embedded processor in an FPGA change the way systems are designed today?

The Virtex-II Pro solution enables a new paradigm in system development with significant benefits, specifically in software engineering productivity. Embedded processors can be used for rapid system pre-production and to allow accelerated software development. A preliminary hardware platform can be built quickly, initially emulated as a C-based algorithm using the embedded processors. This allows software development to be started much earlier in the design process compared to current practice. In addition, software debug can be performed at hardware speeds while the hardware implementation may continue to be speed-optimized. The Xilinx® ChipScope™ on-chip verification tools provide in-system observability into both the FPGA hardware and the processor bus transactions.

How does the Virtex-II Pro solution provide a platform for Architectural Synthesis?

Architectural Synthesis is a combination of tools and technologies that allows designers to specify high-level requirements for their systems for automatic generation of the architecture implementations. This includes a close interaction between hardware and software architectures of the system. The Virtex-II Pro solution offers abundant resources of high performance processors, memory, logic, and other capabilities. With up to 4 processors, this provides a scalable and flexible platform that facilitates hardware-software partitioning for optimal system architecture throughout product development.

What is the value proposition of Virtex-II Pro family?

The close integration of the processors and transceivers into the FPGA fabric results in a very high system throughput at reduced Bill of Materials and manufacturing cost. Instead of using multiple discrete processors and transceivers, the Virtex-II Pro family increases the processing capability while minimizing the number of required I/O pins and reducing the PCB layout complexity.

What applications will the Virtex-II Pro family be able to address?

The Virtex-II Pro family can be used in a wide range of high performance system applications, including optical networking, wireless infrastructure, storage systems and networks, industrial control, broadcast video and image processing. In these applications, the RocketIO multi-gigabit transceiver enables very high-speed end-to-end serial connectivity. With the deeply embedded PowerPC cores, the Virtex-II Pro FPGA provides a powerful platform for complex programmable systems.

What kinds of applications require both processors and transceivers in one device?

Complex programmable systems, such as metro network routers, wireless basestations, and network encryption engines, have a need for high-performance processing and high-bandwidth I/O capability. In these systems, the multiple processor cores require a high rate of data throughput that can only be practical with the new serial I/O standards. Hence Xilinx offers both processors and transceivers on a single Virtex-II Pro device.

What are the members of the Virtex-II Pro family?

It consists of five family members with Block RAM, clock management (DCM), and multipliers. Family members contain anywhere from 4 to 16 RocketIO multi-gigabit transceivers and from 0 to 4 processors, depending on the size of the device.

Device	XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VP50
Logic Cells	3,168	6,768	11,088	20,880	50,832
RocketIO Blocks	4	4	8	8	16
PowerPC Cores	0	1	1	2	4
Block RAM (Kbits)	216	504	792	1,584	3,888
DCM Blocks	4	4	4	8	8
Multipliers	16	40	60	112	264

When will the Virtex-II Pro devices be available?

The XC2VP4, XC2VP7, and XC2VP20 FPGAs are shipping now. All family members will be available in production volume by the end of 2002.

What is the process technology for Virtex-II Pro family?

The Virtex-II Pro family is based on IBM's advanced 0.13 micron, 9-layer copper process technology. In addition to copper interconnect, this process technology utilizes low-K dielectric between layers of metallization, resulting in substantially reduced interconnect delays and higher overall performance.

Where will this family be manufactured?

The Virtex-II Pro FPGAs will be manufactured at IBM and UMC. The initial devices are produced at IBM in Burlington, Vermont.

What is the significance of the new naming convention for this family?

Virtex-II Pro family is part of the Virtex-II series of devices targeted towards applications that can benefit from programmable system level capabilities made possible by the integrated PowerPC processors and RocketIO multi-gigabit transceivers. The Virtex-II Pro part numbers indicate relative device capacity and capabilities among the family members.

What is the volume price of Virtex-II Pro family?

Volume pricing in 2004 will be \$120, \$180, and \$525 for XC2VP4, XC2VP7, and XC2VP20 devices respectively (25,000-unit quantity).

How does Virtex-II Pro FPGA pricing compare with Virtex-II FPGA pricing?

Production pricing for Virtex-II Pro FPGAs will be similar to the Virtex-II FPGAs for comparable logic density and speed. However, the Virtex-II Pro FPGAs provide the added capabilities of embedded PowerPC processors and RocketIO multi-gigabit transceivers, which reduces the Bill of Materials cost.

What types of packages will be available for the Virtex-II Pro family?

The Virtex-II Pro family will be available in cost effective wire-bond packages as well as performance leading flip-chip packages with pin counts ranging from 256 to 1517 pins. The advanced flip-chip packaging technology has a number of performance and reliability benefits including enhanced power supply distribution, signal integrity, and thermal dissipation.

What software is available to support the Virtex-II Pro family?

The Virtex-II Pro family is fully supported in the Xilinx ISE software version 4.2i. For embedded system designs, Xilinx offers an OEM version of WindRiver Systems' tool chain including Diab™ C/C++ compiler, SingleStep™ software debugger and visionProbe-II JTAG for run-control hardware diagnosis. Supporting tools such as VxWorks® RTOS (Real Time Operating System) are available from WindRiver Systems while synthesis and simulation tools are available from leading EDA partners. Xilinx also offers a no fee GNU embedded tool chain.

What IP cores will be available for this family?

Most of the IP cores currently available for Virtex-II devices will be available for the Virtex-II Pro family. Processor specific IP cores such as parameterizable peripherals, including SDRAM/DDR memory controllers, UARTs, IIC controllers, ATM UTOPIA level 2 interface cores are available. Cores that are available initially, using RocketIO as a PHY interface for connectivity standards include 10 Gigabit Ethernet MAC with XAUI and 1 Gigabit Ethernet MAC with gigabit PHY.

What are the key differences between Virtex-II and Virtex-II Pro families?

Even though the Virtex-II Pro family is based on the architecture and features of Virtex-II FPGAs, there are some differences between the two families in addition to the RocketIO multi-gigabit transceivers and PowerPC cores. The ratio of memory-to-logic is higher in Virtex-II Pro as compared to Virtex-II devices. In addition, due to the advanced process technology, the Virtex-II Pro fabric is substantially faster than the Virtex-II fabric.

Will the Virtex-II Pro family replace the Virtex-II family?

No, both Virtex-II Pro and Virtex-II families together form the Virtex-II series Platform FPGAs. The Virtex-II family offers a wide range of densities to meet logic and memory needs. On the other hand with the embedded PowerPC and RocketIO multi-gigabit transceiver cores, the Virtex-II Pro family extends the capability. Many systems will contain both Virtex-II Pro and Virtex-II devices working together.

Is there a migration path to Virtex-II Pro from its Xilinx predecessors?

Xilinx provides a single standard software platform for easy migration and upgrade from Virtex, Virtex-II families to Virtex-II Pro family.

What is the competition?

Up to this point, many designers had to rely on standard cell technology in order to achieve the performance and integration necessary to implement complex high performance systems. Virtex-II Pro FPGA now fulfills the same requirement with added programmable flexibility.

FPGAs with embedded processors to date have limitations in the number of processor cores available and processing performance. The Virtex-II Pro architecture is unique in providing multiple processor cores per device, which are needed for the most challenging programmable system implementations. As well, it is the only FPGA using the PowerPC architecture, the most popular embedded processor, offering twice the processing performance of other embedded processors. Unlike other FPGA products with embedded processors, the Virtex-II Pro product is targeted for mainstream production, rather than low-volume ASIC prototyping for consumer applications.

Systems designers are looking for a platform for emerging connectivity solutions, not just transceivers on an FPGA. Having embedded processor cores on-chip reduces the required logic to implement these new connectivity standards. Other programmable products with embedded clock/data recovery fall short in serial data rate or FPGA logic resources. None of those products contain embedded processors for handling complex emerging protocols.

HIGH-SPEED SERIAL TRANSCEIVERS

What technology is used in the RocketIO multi-gigabit transceivers?

The RocketIO multi-gigabit transceivers in Virtex-II Pro devices are based on the latest SkyRail™ transceiver technology from Mindspeed Technologies (a Conexant business). SkyRail™ transceivers have been proven both in performance and manufacturability, demonstrating 3.125 Gb/s transfer rates on devices fabricated using standard CMOS process.

What emerging IO standards do RocketIO multi-gigabit transceivers enable?

The RocketIO technology within the Virtex-II Pro family supports several emerging serial standards including InfiniBand, 10 Gigabit Attachment Unit Interface (XAUI), Gigabit Ethernet, Serial ATA, Fibre Channel – FC2X, 4X, 10X, RapidIO Serial, and Arapahoe/3GIO. The unique channel bonding capability of RocketIO multi-gigabit transceiver enables bonding together multiple channels for high aggregate bandwidth up to 40 Gb/s per device.

What are the benefits of using RocketIO blocks instead of discrete SerDes devices?

A single discrete Quad 3.125 Gb/s SerDes requires more than 100 interface pins within a 340-pin BGA package. The integration of multiple Quad SerDes into a single Platform FPGA eliminates hundreds of interface signals and several extra components. The result is less board area, fewer board layers, reduced component count, reduced FPGA pin-count, and higher reliability.

How does Virtex-II Pro enable bridging across multiple varying standards?

The Virtex-II Pro family supports both high bandwidth parallel and serial standards. The RocketIO and the SelectIO-Ultra technologies (part of the SystemIO solution) enable bridging of existing parallel standards to emerging multi-gigabit serial standards.

THE IBM POWERPC 405GP

Why did Xilinx choose the PowerPC processor architecture?

The PowerPC architecture has wide acceptance in performance-oriented applications, as well as comprehensive third-party tool support. PowerPC processor is the standard in networking and communications systems. According to Dataquest (July 2001), the IBM PowerPC architecture holds the

largest share of all embedded processor market and has experienced the highest year-to-year growth from 1999 to 2000 in embedded system space.

Which PowerPC core is embedded in the Virtex-II Pro family?

The Virtex-II Pro architecture uses the PowerPC 405 processor core. The exact implementation is a 0.13-micron migration of the proven 0.18-micron PowerPC 405D4 core from the IBM Blue Logic™ core library.

What percentage of the die area does the processor occupy?

Each PowerPC 405 core takes up as little as two percent of the total die area providing ultimate performance and functionality for the area occupied. For complex computational intensive system designs, the PowerPC cores offer significant area savings over the equivalent FPGA logic implementations.

Why did Xilinx embed multiple processors?

Leading edge systems comprise of multiple independent subsystems. These systems can be optimally partitioned using multiple processor-based implementations. For example, high-end networking systems today consist of a central processor for system processing and multiple communications processors for control plane functions. Virtex-II Pro architecture provides up to 4 PowerPC processors to enable such systems.

What is the CoreConnect bus technology?

The IBM CoreConnect bus is a high-speed bus architecture that enables easy integration and design reuse of peripheral cores. It comprises of the processor local bus (PLB) for high-speed peripherals, the on-chip peripheral bus (OPB) for general-purpose peripherals, and device control register (DCR) bus for system control. Both the PowerPC processor and the MicroBlaze soft processor support the CoreConnect bus.

What are the key benefits of FPGA architecture with embedded processors?

Embedded processors within Platform FPGA architectures extend the capability of programmable logic to the realm of programmable systems. Many complex applications comprise speed-intensive raw-data processing and control-intensive system management. All such applications can be optimally partitioned into separate, but tightly integrated FPGA logic and embedded processor sections, depending on the speed vs. complexity tradeoff in the hardware/software continuum.

What are the benefits of using the embedded processor cores instead of external processors?

Processor cores deeply embedded into Platform FPGA fabric with tightly integrated input/output signals provide the following key benefits over external processors:

- Enable high data transfer between processor and fabric
- Enable flexible and scalable processor peripherals
- Reduce system development and debug time
- Lower Bill-of-Materials costs

ENABLING PARTNERSHIPS

Why is this an “Industry-developed, Xilinx delivered” solution?

Industry leaders in each field including IBM, Mindspeed, WindRiver Systems, UMC, and Xilinx jointly worked together on various facets of the underlying technologies to create the Virtex-II Pro Platform FPGA solution. In addition, leaders in EDA, verification, IP development, and network connectivity

worked together to support the Platform. This is not just a product but a complete solution with an industry ecosystem built around it making it an industry-developed, Xilinx delivered solution.

What is the agreement between IBM and Xilinx?

IBM and Xilinx signed a broad-based technology agreement. This agreement enables the creation of advanced FPGA products that incorporate the PowerPC and CoreConnect bus technologies from IBM with FPGA technology from Xilinx. It also allows Xilinx to leverage IBM's industry leading manufacturing process, a foundry resource, and an expertise in system development.

What is the partnership agreement between Mindspeed Technologies and Xilinx?

Xilinx licensed the proven SkyRail™ CMOS transceiver technology from Mindspeed Technologies (a Conexant business).

What is the partnership agreement between WindRiver Systems and Xilinx?

Xilinx has an OEM agreement with WindRiver Systems on embedded software tools including compiler, software debugger, and hardware probe. In addition, WindRiver Systems has ported their VxWorks RTOS and other tools for the Virtex-II Pro solution.

What is the FPGA market share for Xilinx?

Xilinx has over 90% market share for advanced architecture FPGAs, which include the Virtex, Virtex-E, and Virtex-II families, based on publicly disclosed revenue numbers. The advanced architecture FPGAs are those that integrate system level features such as a wide range of input/output standards, clock generation circuitry, block memory and very high logic gate counts.