**Xilinx Virtex-4 Revolutionizes Platform FPGAs**

**The Rise of Platform FPGAs**

Xilinx introduced the concept of a Platform FPGA as its Virtex family found increased use in system-on-a-chip (SoC) applications. As the leading programmable logic vendor, Xilinx helped to usher in and establish the SOC design methodology with its capable Virtex-based device support of programmable logic, I/O, and processing. Xilinx had already established itself with numerous implementations of FPGA-based RISC processors and processor cores, with the earliest example being Philip Freidin’s RISC4005/R16 FPGA processor implementation in 1991. The Platform FPGA concept was fully realized with the introduction of the Virtex-II PRO™ PowerPC hard processor and MicroBlaze soft processor core’s support of all Virtex FPGAs.

Platform FPGAs quickly took over innumerable ASIC SoC designs with its flexible device integration capability, programmable I/O, very capable clock speed, and significantly lower overall design cost. The addition of high-performance RISC CPUs, block RAM, multi-gigabit high speed serial I/Os, dedicated DSP logic, and other system enhancements introduced technological advances which further solidified the rise of Platform FPGAs over their ASIC SoC counterparts.

**Architectural Advantage**

To give its next generation Virtex-4 family every advantage and significantly lower its cost structure, Xilinx created a new architecture framework — the Advanced Silicon Modular Block (ASMBL) architecture. The ASMBL architecture being the basis for the fourth-generation Virtex FPGAs (Virtex-4) enables Xilinx to cost-effectively develop multiple FPGA platforms, each with different combinations of feature sets. As a result, Virtex-4 expands Platform FPGAs into revolutionary new silicon territory with combinations of both advanced and architecturally unique capabilities. For the first time in the history of FPGAs, the ASMBL architecture allows multidimensional application scaling based on required features and/or cost.

This revolutionary concept enables the creation of distinct functional platforms, whose ratio of base features defines their domains. In the case of the Virtex-4 FPGA family, initially three platforms will target four application domains—a Logic Domain, a DSP Domain, a Connectivity Domain, and an Embedded Processing Domain. Each platform will have different sized devices with approximately the same feature-set ratio as other devices in the same platform. Each device maps into separate application segments and sub-segments depending on its cost parameters and desired function. This application mapping process means a standard platform device can match a wide variety of specific applications.

The need for different platform FPGA devices with optimized feature sets is clear, yet the resulting device need not be application specific. Such platform FPGA devices allow multidimensional application scaling by their ability to match both cost parameters and functional feature sets to a wide range of divergent applications. In addition, exclusive use of advanced flip-chip packaging provides distinct power and ground distribution advantages that are important when using 90nm technology as well as significantly improving a platform device’s programmable routing capability. This means a specific device can be tailored to best meet the widest range of application requirements typically delivered by ASICs, ASSPs, and similar devices in the most cost-effective manner.
The “Total Cost” Advantage
A substantially higher cost and longer design times for state-of-the-art ASICs and ASSPs relegates their primary uses to proven, lower-risk, very-high-volume applications. The rapid and significant increase in ASIC development costs clearly tips the advantage to using increasingly capable platform FPGAs in both bleeding- and leading-edge applications, something Xilinx will continue to exploit in future-generation device families. The simultaneous introduction of three platforms radically increases design choices to meet a particular price point and is sure to accelerate Platform FPGA expansions into even more application areas.

The unexpected, or less obvious aspect, behind an FPGA capturing an initial design win is that projected target volumes often don’t reach a point to justify a conversion of an FPGA design to ASIC or standard-cell technology. The overall cost benefit of zero NRE pushes the high-volume ASIC or ASSP crossover point upwards, locking in FPGAs like never before. Customers finding themselves with a fixed higher volume design can use Xilinx’s EasyPath program to further reduce device cost in volume production by 25% to 75%. EasyPath utilizes a custom-device test file to test and pass only used device resources, logic, and interconnect used by the high-volume design files. This reduces test time and increases yield, lowering overall cost that is passed on to the customer, and it provides customers with a no-risk migration to a lower cost solution.

The trend showing fewer ASIC design starts and an increase in FPGA design wins over time is well established in articles by industry news sources and reports from iSupply, Gartner Dataquest, and others. Next-generation platform FPGA devices will greatly expand silicon-processing options and will continue to push ASIC design starts lower as additional application domains are defined and more revolutionary devices are introduced.

A Decade of Progress
The exponential increase in Xilinx FPGA’s capabilities over the last decade shows the dramatic impact the Virtex-4 family brings -- over a 250x increase in device capacity, a 25x increase in clock frequency, over an 800x increase in memory bandwidth, and a 1000x increase in I/O bandwidth. Normalizing device cost results in a 300x reduction in price. The popularity of FPGAs over alternative silicon solutions is a clearly demonstrated trend; DSP and RISC processor vendors admit that > 80% of board-level designs incorporate FPGA devices to provide the necessary system level design flexibility.

A primary goal in the developing the ASMBL architecture and the resulting Virtex-4 family is one of simple economics. FPGAs have demonstrated a clear and consistent trend in reducing cost and making FPGA technology more suitable for a wider range of applications. A key and often overlooked component in the economic picture is clearly demonstrated in how technology is used throughout the world; no two people use the same technology, systems, or software, nor do they subscribe to or want the same content. The resulting picture suggests evolvable hardware enables a mass market of one. Virtex-4 further extends the concept of evolvable hardware within the cost confines of a standard product—or in this case, a single Virtex-4 family with multiple platforms.

ASMBL’s Cookie-Cutter Model
What makes the most sense with the ASMBL architecture is the design efficiency behind making a small number of functionally specific 90nm silicon columns (the hard work) and then efficiently reusing them (simple work) to create a wide range of devices. The Xilinx designers can vary the number and ratio of
different functional columns to create a platform or family of different sized devices, each best suited for a certain domain of applications depending on the desired type of functional attributes. It is important to note that, like current platform FPGA devices, a domain-optimized family doesn’t restrict that family’s use to a certain application space, since the device’s inherent flexibility allows its use in many different applications.

**Virtex-4: One Family -- Multiple Platforms**

Xilinx used an elaborate process to define an optimized set of features to best meet specific customer-application requirements. The grouping defined predominate processing architecture types and resulted in application domains described as logic, DSP, connectivity, and embedded processing. The ratio of basic features in all four domains could be satisfied with three platforms.

Common to all the Virtex-4 Platform FPGAs is the traditional highly flexible “programmable logic” with its programmable interconnect and I/O structures. What becomes unique to a particular platform is how the “logic” is used together with other specialized functions such as RAM, DSP blocks, and I/Os. Mixing features in different proportions creates a platform or domain that is best suited and optimized for certain types of general processing tasks across a broad range of applications. Other enhanced features in the Virtex-4 family included new Digital Clock Management (DCM) with differential clock tree, new and faster block RAM that can be configured as FIFO, enhanced PowerPC 405 core with an Auxiliary Processor Unit (APU) for direct interface between CPU and fabric, 1Gbps parallel I/O with improved source synchronous interface capabilities, 0.6 – 11.1 Gbps serial transceivers with flexible DFE receiver equalization, and an enhanced XtremeDSP slice with built in Multiply and Accumulate (MAC) functionality for highest possible signal processing performance. System features are performance matched to 500 MHz clock to eliminate any bottleneck in a system design.

**Domain-Optimized FPGA Platforms**

The Virtex-4 family is introduced with three platforms; LX for highest performance and density logic integration, SX for highest performance signal processing applications and FX for full-featured processing and connectivity SoC designs. A device from any of the three platforms can be ideal for a large number of applications depending on cost and performance requirements. The platforms are optimized for a target domain, or class of applications, however all types support many applications.

An application or its processing architecture can favor a particular platform, but that doesn’t mean it’s always the best fit. A good example is that implementation of algorithms in logic might look to favor logic-centric (LX) platforms, but these same algorithms can also be implemented in a DSP (SX) or system (FX) device. In a similar fashion, the need for an application to have a simple control processor isn’t restricted to a system-domain device (FX). With a soft processor core such as MicroBlaze the processor can be implemented in either a DSP (SX) or logic (LX) device.

**Virtex-4 LX -- Logic Optimized Platform**

The most general-purpose family would be the Virtex-4 LX or logic optimized platform family. The LX family is similar in function to early Virtex-II devices without the embedded PowerPC processor or higher-speed serial I/Os found in the newer Virtex-II Pro™ devices. All types of soft Intellectual Property (IP) cores can be implemented on this Platform, including various DSP blocks and soft processor cores.
such as MicroBlaze or PicoBlaze. The primary benefit is the use of highly integrated general-purpose logic elements, which makes this the most cost-effective logic platform.

The Virtex-4 LX Platform will have several family members with small-to-large-size devices, making it a suitable match for many applications. This family will have twice the logic density of any device shipping today. The cost benefits of using advanced 90nm silicon fabrication technology on 300mm wafers, together with cost-effective device packaging insures this platform’s broad-based acceptance. The higher clock frequencies compared to previous generation platform FPGAs greatly expands the LX Platform’s suitability for replacing ASICs.

**Virtex-4 SX -- Signal Processing Optimized Platform**

Increasing the ratio of DSP and memory blocks to the number of logic elements creates the Virtex-4 SX, or signal-processing/DSP Platform family of devices. The changed ratio of features creates a relatively smaller die size Platform in comparison to other Virtex-4 platforms for high-speed signal processing. This tradeoff combined with the new DSP slice features packs the capability for the highest DSP performance into the most cost-effective Virtex-4 SX Platform.

With significantly higher DSP bandwidth at much reduced power consumption of previous Virtex-II Pro devices, the Virtex-4 SX Platform delivers the most DSP performance per dollar compared to any other device. Each DSP Slice implements an 18-bit x 18-bit MAC that can be clocked at 500MHz. The impact of Virtex-4 DSP specific enhancements to include new modes and capabilities, together with other parts of the optimized SX Platform architecture, enables more capable higher level DSP IP.

**Virtex-4 FX -- Full-Featured Platform**

Adding a PowerPC and high-speed serial transceivers creates the full-featured Virtex-4 FX platform. The combination of features, architecture, and fabrication process enables processor clock speeds of up to 450 MHz. Combining this capability with serial transceivers supporting any speed from 600 Mbps to 11.1Gbps provides a very capable high-performance platform FPGA that meets embedded-processing and connectivity-domain requirements.

The FX Platform incorporates advanced system features that are particularly useful in a wide-range of applications in the Telecom, Storage, and Networking space, and other system applications requiring high-performance processing and high-bandwidth I/O. These applications can be segmented into two general application domains based on the system behavior. The embedded-processing domain is dominated by control flow operations involving complex data types. The connectivity-domain involves message-based processing and is dominated by asynchronous data flow operations. Both domains are best implemented on the Virtex-4 FX full-featured platform.

**Complete System Connectivity Platform**

The entire Virtex-4 family has a diverse set of programmable I/O capabilities that makes it a complete system connectivity platform. In addition, Xilinx pioneered a wide range of new industry standards, for example by founding the UXPI Standards Organization (See www.uxpi.org). The Virtex-4 Connectivity Platform builds on the groundbreaking success of the Virtex-II Pro with its implementation of PCI Express Advance Switching (AS) specification in conjunction with the Advanced Telecom Computing Architecture (ATCA or AdvancedTCA™) Initiative.
The Virtex-4 FX Platform is particularly well suited to higher-end, yet cost effective systems that must use the latest in high-speed serial backplane technology. The combination of worry-free black box IP, the very capable Virtex-4 FX Platform, and its broad-based standards bodywork makes Xilinx a key player in setting new I/O Standards for the industry. For example, Xilinix is playing a critical role in combining AdvancedTCA™, carrier-grade Linux, and PCI Express AS on Virtex based development platforms easing the development of full-mesh fabric solutions. Xilinx's eSP Web portal featuring the latest Virtex Connectivity Platform is serving as the key enabler of the industries most advanced I/O technology.

**Leading Application-Adaptable IC Technology**

Increasing demand for greater application adaptability at cost-effective price points is prompting concurrent introduction of three separate Virtex-4 platforms. The new Virtex-4 Platform FPGAs maximize function and value. Users are able to incorporate a wide variety of soft-IP and multiple processor cores.

Customer feedback shows users are ready and able to make smarter and more efficient use of programmable fabrics for various co-processing functions, including in-the-field adaptability to changing performance or feature requirements. The universal appeal of such a flexible silicon platform offered in the Virtex-4 family dramatically expands the role for FPGAs in a wide range of system designs.

Designers have never had such control or choice in the type of application processing that is offered in Virtex-4 Platforms. The flexibility in implementing a wide-range of processing functions is unparalleled—implementing any combination of processing functions on a PowerPC, in a co-processor, or in direct implementation of an algorithm in hardware provides tremendous flexibility. Designing the right level of performance into control and data structures can eliminate the traditional boundaries between segmented control and data planes.

The unique flexibility and ability to create optimal application domain subsystems using multiple Virtex-4 Platforms sets even higher standards for FPGAs. Devices that are both hardware and software programmable enable more flexible implementation options than either ASIC or ASSP devices.

**Shifting Architectural Exploration and Design Process**

The fixed nature of the traditional system and ASIC design process was turned upside down with the introduction of increasingly capable Platform FPGAs. The value proposition with Virtex-4 FPGAs is clear; they deliver the highest capability at the lowest cost. In addition, these devices and their associated tools have a significant impact on the silicon platform development process. The ability to reinvestigate and change or enhance system architecture any time in the development process gives designers the ultimate toolkit to meet application requirements. This flexibility becomes paramount in the situation of emerging or competing standards. The same capability can be used to evolve hardware in the field to meet new requirements or avoid expensive hardware upgrades. The Virtex-4 family provides the greatest in-field flexibility by allowing any combination of hardware and/or software upgrades.

All phases in the design process benefit from the enhanced instrumentation capability offered in Virtex FPGAs. This capability is unique to FPGAs and allows the insertion of bus or logic analyzers anywhere
in the design. Although typically this capability is removed in final shipped product, the capability still exists if it is needed to troubleshoot complex customer problems or enhance performance.

**Process Technology Leader**

Xilinx clearly demonstrates process technology leadership by being one of the very first fabless semiconductor companies to sample products based on advanced 90nm silicon technology early in 2003. Xilinx gained significant silicon fabrication experience as an early adopter of 300mm (12-inch) wafer technology, shipping over three million units using this advanced technology. The Virtex-4 family uses both 90nm technology and 300mm wafers to give it distinct cost advantages.

The combination of using 90nm silicon fabrication technology together with 300mm wafers results in a cumulative effect of increasing the number Virtex-4 die per wafer 5 times over the previous Virtex-II generation FPGAs. Increasing the die per wafer together with Virtex-4 architectural integration enables substantially lower system cost.

Effective use of 11 metal layers is an important enabler of the ASMBL architecture, as it enhances the on-chip routability to support the column-based modules. Enhanced routing combined with dispersed I/O structures are key elements of the Virtex-4 platforms.

**Conclusion**

The new Virtex-4 FPGAs are revolutionary in their ability to accelerate the deployment of FPGA technology into many more domain-optimized application areas. Not only does a designer or design team have choices in selecting the ideal platform, but also a choice in picking the size of device to best achieve needed capability. The focus of the Virtex-4 family is clearly to enable use of FPGAs in new and multiple application-domain spaces, while best serving the needs of existing FPGA customers. There are additional advantages in being able to learn one lower cost tool set, design methodology, and architectural feature set. Most importantly, the next-generation Virtex-4 delivers significantly higher capability at the lowest cost. Virtex-4’s multiple platforms will lead all FPGAs in logic density, DSP and processing performance, and I/O bandwidth.