

# DESIGNCON<sup>®</sup> 2014

13-TU1, Tuesday Jan 28<sup>th</sup>, 1<sup>st</sup> Speaker 9:00 am to 9:20

## 28 Gb/s SERDES Channel Overview

Jack Carrel

Romi Mayder

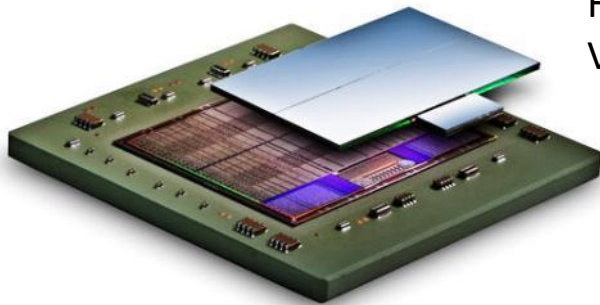
 XILINX  ALL PROGRAMMABLE<sup>™</sup>

January 28-31, 2014 | Santa Clara Convention Center | Santa Clara, CA

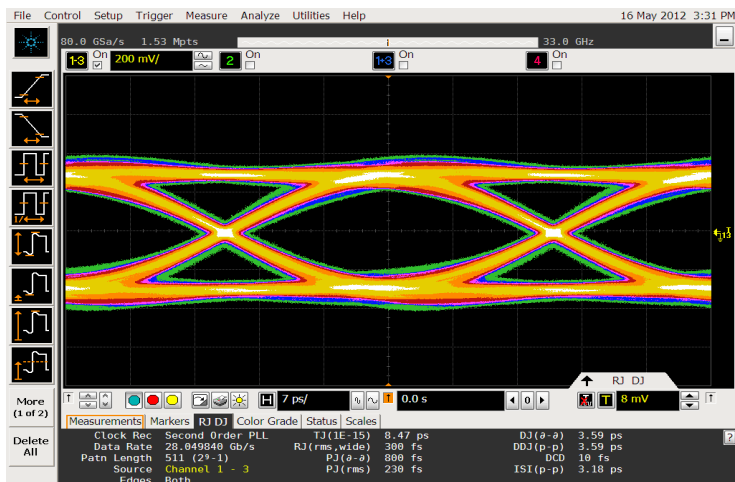
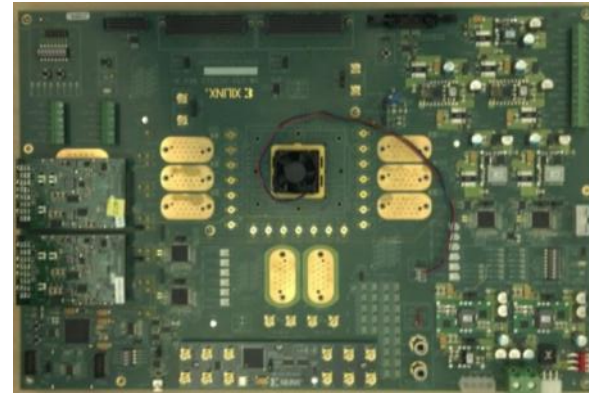
# Introduction

- SerDes links running at 28Gb/s
- Understanding performance at device pin is important
- Need to characterize the transmitter at device pin
- Measurement is dependent on Channel Fixture
  - PCB Channel
  - Connectors
  - Cables
- Channel Fixture de-embedding required to observe launch waveform

# 28nm FPGA with GTZ XCVR 7H580T

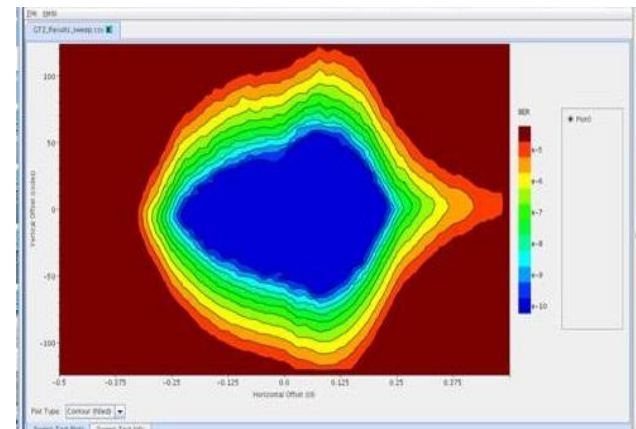


Heterogeneous  
VH580T



VH580T GTZ TX

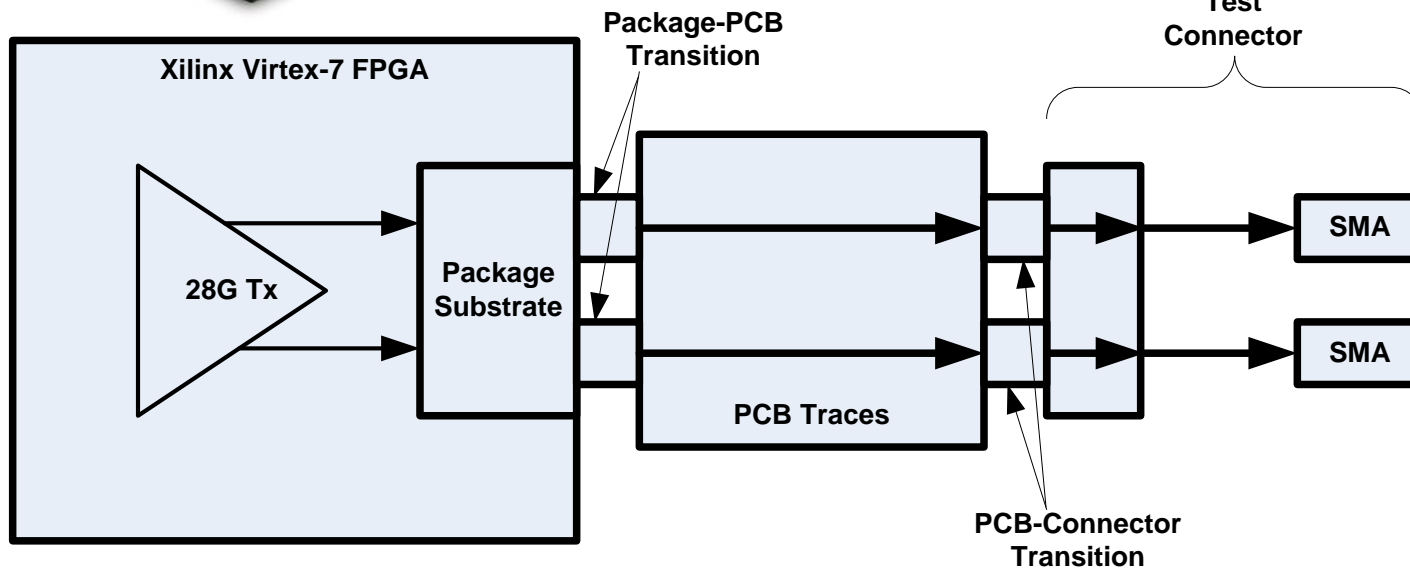
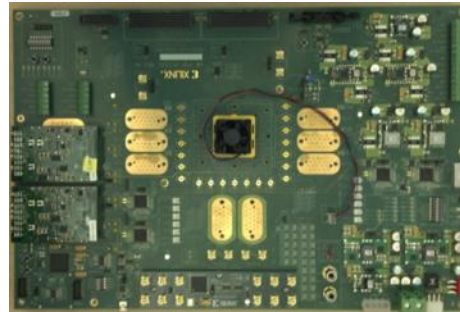
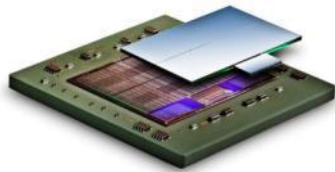
Eye Diagram: 28.05Gb/s



VH580T GTZ

RX Eye Scan: 28.05Gb/s:  
Thru 12.5dB Trace

# 28G Fixture Channel





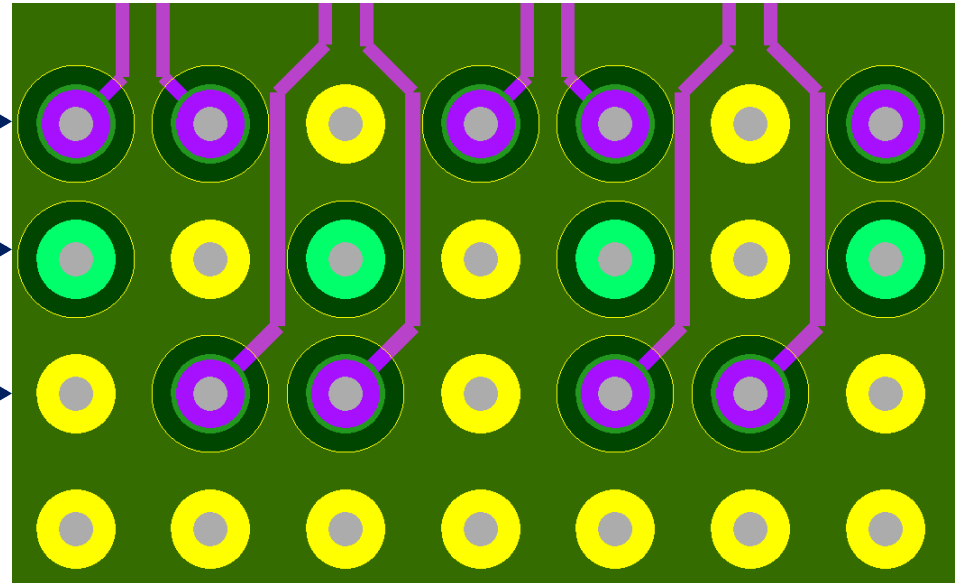
# Physical Description PCB Stackup

- 22 Layers
- HS signal layers: Panasonic Megtron6
- Other layers: ISOLA 370HR - FR4
- For Megtron6 and 370HR interleaved in lower layers for mechanical stability
- For economic reasons other layers are standard FR4 (ISOLA 370HR)

Layer	Type	CU Weight	CU %	Material Description	Via Structure	Segment
Soldermask						
1	Signal	H	20	Press thk = 4.56 mil		Foil
2	Plane	H	94	3.9 mil H/H		Prepreg
3	Signal	H	20	Press thk = 5.38 mil		Core
4	Plane	H	94	3.9 mil H/H		Prepreg
5	Signal	H	5	Press thk = 5.29 mil		Core
6	Plane	H	94	3.9 mil H/H		Prepreg
7	Signal	H	5	Press thk = 5.29 mil		Core
8	Plane	H	94	3.9 mil H/H		Prepreg
9	Mixed	H	9	Press thk = 5.32 mil		Core
10	Plane	H	94	3.0 mil H/H		Prepreg
11	Plane	H	91	Press thk = 5.31 mil		Core
12	Plane	H	94	3.0 mil H/H		Prepreg
13	Plane	H	89	Press thk = 5.78 mil		Core
14	Plane	H	91	3.0 mil H/H		Prepreg
15	Plane	H	94	Press thk = 5.50 mil		Core
16	Mixed	H	39	4.0 mil H/H		Prepreg
17	Plane	H	94	Press thk = 5.28 mil		Core
18	Signal	H	3	4.0 mil H/H		Prepreg
19	Plane	H	94	Press thk = 5.28 mil		Core
20	Signal	H	3	4.0 mil H/H		Prepreg
21	Plane	H	94	Press thk = 4.56 mil		Core
22	Signal	H	21			Foil
Soldermask						

# Physical Description Pin/Via Breakout

- Highspeed Signal Pin pad (Backdrilled) →
- Standard Signal Pin pad (not Backdrilled) →
- Ground Via (Not Backdrilled) →

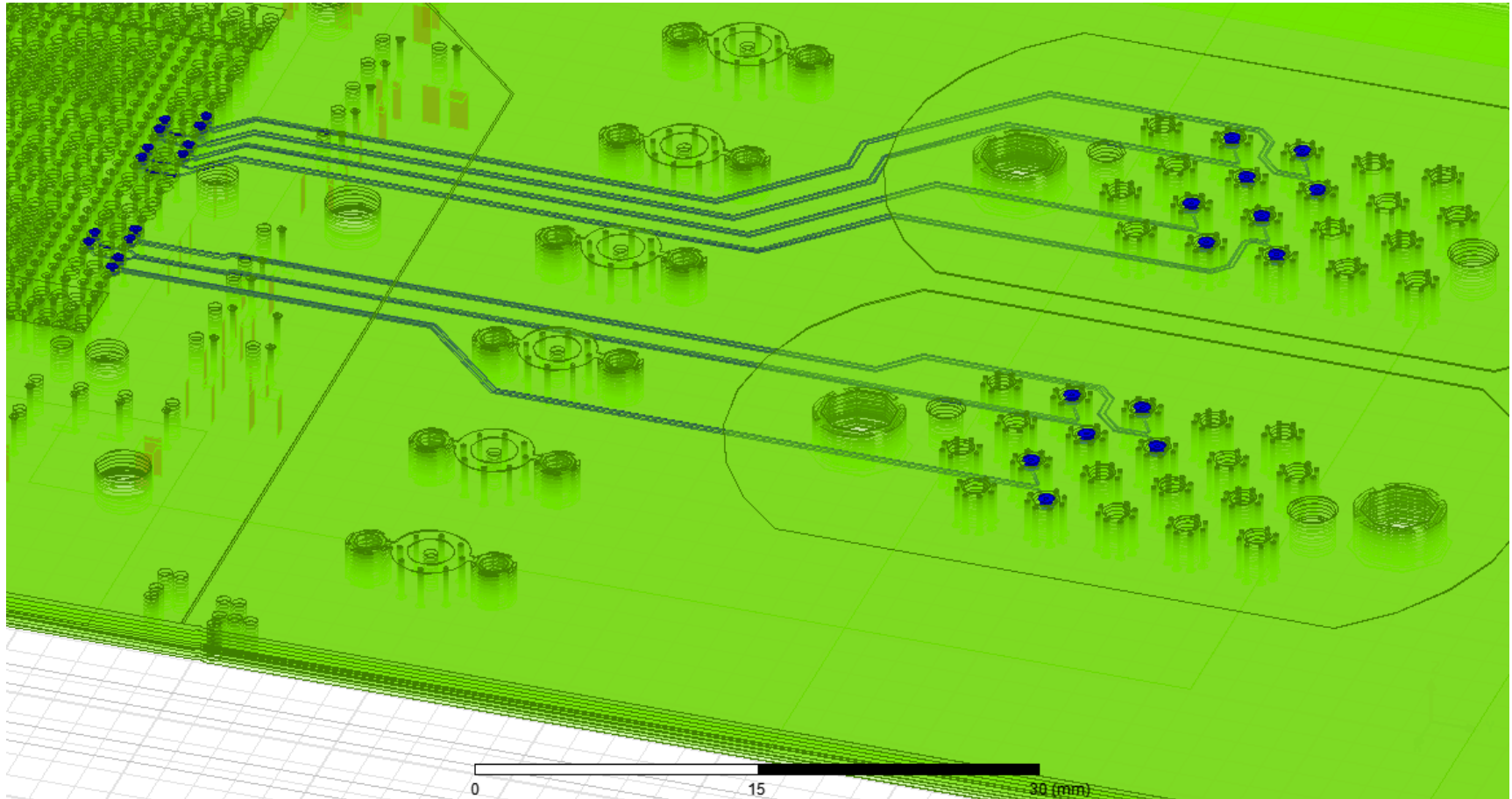


## Vias

- 10 mil Drill
- 20 mil pad
- 28 mil anti-pad

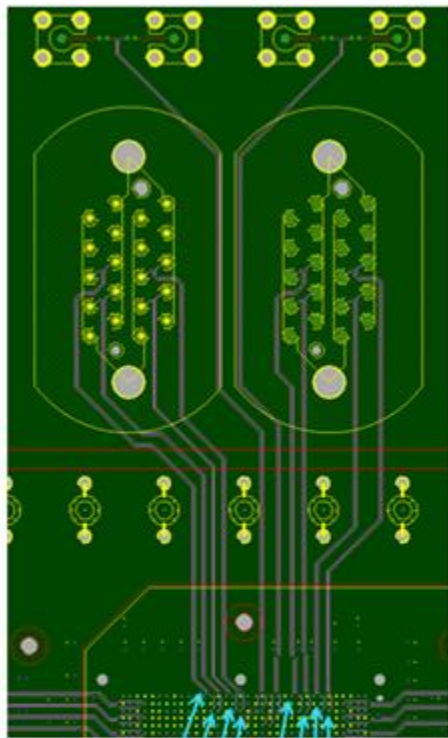
Backdrill – 8 mils of target layer +/- 3mils

# Physical Description PCB Layout





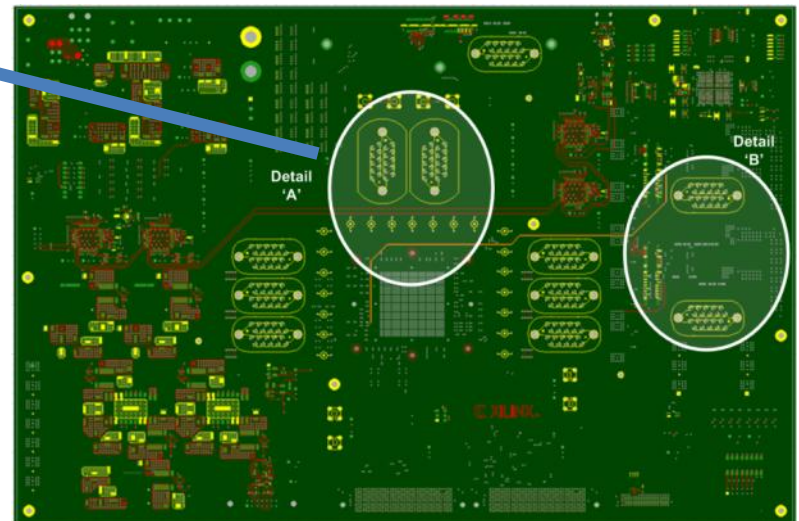
# Channel/Physical - PCB



Detail 'A'

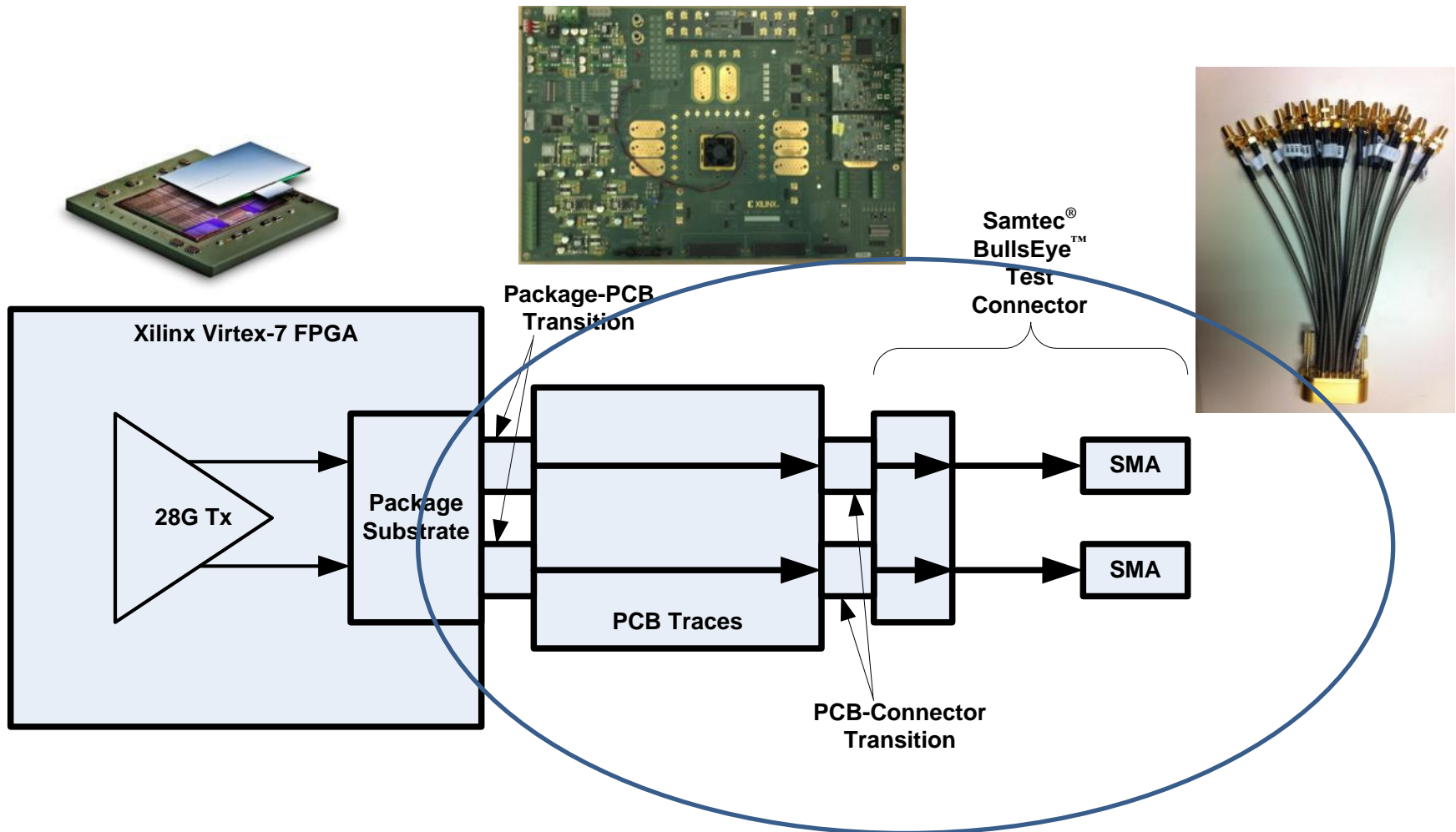
TX7  
TX6  
TX5  
TX4  
TX3  
TX2  
TX1  
TX0

Net	Etch Length (in)	Routing Layer	Trace Width (mil)	Trace Spacing (mil)
TX0	2.683	5	3.75	8.25
TX1	2.293	5	3.75	8.25
TX2	2.298	5	3.75	8.25
TX3	2.501	5	3.75	8.25
TX4	2.698	5	3.75	8.25
TX5	2.373	5	3.75	8.25
TX6	2.607	5	3.75	8.25
TX7	2.804	5	3.75	8.25





# Fixture De-Embed Challenge



# Next Speaker

- **28 Gb/s SERDES Channel Overview – Romi Mayder and Jack Carrel (20min)**
- **Fixture S-parameter model from 2x Fixture Physical Test Structures – Mike Resso (35 min)**
- **Fixture S-parameter model from Simulated Measurement Based Model – Heidi Barnes (35 min)**
- **Waveform Measurements at the DUT using S-parameter model de-embedding. Rob Sleight (1 hour)**
- **Lessons Learned – Jack Carrel (15 min)**