Zynq®-7000Q Defense-grade All Programmable SoCs

XILINX.

	Device Name	Z-7020		Z-7030		Z-7045		Z-7100	
	Part Number	XQ7Z020		XQ7Z030		XQ7Z045		XQ7Z100	
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™							
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor							
	Maximum Frequency	733 MHz							
	L1 Cache	32 KB Instruction, 32 KB Data per processor							
	L2 Cache	512 KB							
	On-Chip Memory	256 KB							
	External Memory Support	DDR3, DDR3L, DDR2, LPDDR2							
	External Static Memory Support	2x Quad-SPI, NAND, NOR							
	DMA Channels	8 (4 dedicated to Programmable Logic)							
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO							
	Peripherals w/ Built-in DMA	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO							
	Security[1]	AES and SHA 256b Decryption and Authentication for Secure Boot							
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts							
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7Q FPGA		Kintex®-7Q FPGA		Kintex-7Q FPGA		Kintex-7Q FPGA	
	Programmable Logic Cells (Approximate ASIC Gates[2])	85K Logic Cells (~1.3M)		125K Logic Cells (~1.9M)		350K Logic Cells (~5.2M)		444K Logic Cells (~6.6M)	
	Look-Up Tables (LUTs)	53,200		78,600		218,600		277,400	
	Flip-Flops	106,400		157,200		437,200		554,800	
	Extensible Block RAM (36 Kb Blocks)	560 KB (140)		1,060 KB (265)		2,180 KB (545)		3,020 KB (755)	
	Programmable DSP Slices (18x25 MACCs)	220		400		900		2,020	
	PCI Express® (Root Complex or Endpoint)	—		Gen2 x4		Gen2 x8		Gen2 x8	
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs							
	Security[1]	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration							
Speed Grades	Q-Temp (–40°C to 125°C)	-1		-1		-1, -1L		NA	
	Industrial (–40°C to 100°C)	-1, -1L, -2		-1, -2, -2L		-1, -2, -2L		-1, -2, -2L	
Packages	Package Type[3]	**CL400**	**CL484**	**RB484[5]**	**RF676**	**RF676[6]**	**RF900**	**RF900**	**RF1156**
	Size (mm)	17x17	19x19	23x23	27x27	27x27	31 x 31	31x31	35x35
	Pitch (mm)	0.8	0.8	1.0	1.0	1.0	1.0	1.0	1.0
	Processing System User I/Os (excludes DDR dedicated I/Os)[4]	54	54	54	54	54	54	54	54
	Multi-Standards and Multi-Voltage SelectIO™ Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	125	200	100	100	100	212	212	250
	Multi-Standards and Multi-Voltage High Performance SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V)	—	—	63	150	150	150	150	150
	Serial Transceivers	—	—	4	4	8	16	16	16
	Maximum Transceiver Speed (Speed Grade Dependent)	N/A	N/A	6.6 Gb/s	10.3125 Gb/s	10.3125 Gb/s	10.3125 Gb/s	10.3125 Gb/s	10.3125 Gb/s

XMP092 (v1.2)

Notes:
1. Security block is shared by the Processing System and the Programmable Logic.
2. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.
3. Devices in the same package are footprint compatible.
4. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. In that case, the designer can use the Programmable Logic SelectIO™ interface.
5. RB484 is a ruggedized version of FB484 (4-corner lid added) and the RF packages are ruggedized versions of the FF packages
6. The XQ7Z045-RFG676 Pb-free devices are available in the -1Q and -1LQ speed grades.
7. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.