MASSIVE DATA ACQUISITION WITH SPARTAN ULTRASCALE+ FPGAs

AMD
SPARTAN
UltraScale+

OVERVIEW

The continuous processing of data from and to sensors and actuators is key for condition monitoring as well as health management of machines. Information often comes through dedicated ports with specific protocols. A voltage swing of 3.3V is a common characteristic of distributed data sources.

MCUs and SoCs often have I/O-related limits, making FPGAs the optimal solution for connectivity that exactly matches the target application. Customization through programmability is where FPGAs excel. Intelligent solutions have higher value with next devices, which have sufficient ports with a wide enough range of voltages and speeds in combination with integrated memory and programmable logic for algorithms for automation.

AMD has a long history with scalable FPGAs that bring flexibility into product architectures. The new Spartan™ UltraScale+™ family brings connectivity to the next level with:

- Highest I/O-to-logic-cell ratio[1] in the FPGA Cost-Optimized Portfolio
- A wide range of I/O voltages up to 3.3V as single-ended LVTTL and LVCMOS I/O
- High-performance I/Os with up to 2.5G data rate for single-ended and differential interfaces with LVDS, HSTL, and SSTL
- Built-in memory controller for LPDDR4x and LPDDR5 with data rates up to 4266 Mb/s
- Transceivers up to 16.3 Gb/s and built-in hardened PCIe® up to Gen4 x8

HIGHLIGHTS

POWER CONSUMPTION IMPROVEMENTS

- Optimized I/O-to-logic-cell ratio keeps silicon size small
- Hardened blocks for PCIe and DDR memory control reduce power consumption[2]
- Up to 30% less power[3] than with 28 nm FPGAs

ADVANCED SECURITY FEATURES

- Developed with state-of-the-art security features such as PQC with NIST-approved algorithms, on-chip AES-GMC decryption, the physically unclonable function for device uniqueness, and a true random number generator
- AMD's UltraScale+ Portfolio has lower soft error rates (SERs) from single event upset (SEUs) compared to AMD devices in larger technology nodes[4]

DSP BLOCKS

- Provide support of up to 27 x 18 multipliers in a DSP slice and 35 x 28 multipliers in a DSP tile
- Include 24 slices in the smallest device and 384 slices in the largest devices
- Help to meet real-time requirements with advanced control algorithms

LONG PRODUCT LIFETIME

- Spartan UltraScale+ FPGAs are designed for 15-year product lifecycle
- Lengthy product lifecycle support with the option for secure updates

KEY APPLICATIONS

AGGREGATION OF SENSOR DATA

- Condition-based monitoring in automation
- Connectivity using standard protocols like I^2C, SPI, Industrial Ethernet, and proprietary protocols enabled through commercially available IP cores
- Block RAM and UltraRAM allow streaming data into on-chip memory; external DRAM with LPDDR4 and LPDDR5 is supported in select devices

SCALABLE NETWORKING FRONTEND

- Ideal for Industrial IoT with MicroBlaze™ V processor and Ethernet MAC as soft IP cores
- TSN, EtherCAT, Profinet, and EtherNet/IP
- Security features to help reduce vulnerabilities

SAFE I/O AND CONTROL ARCHITECTURES

- UltraScale+ portfolio and the AMD design tools are targeted for certification per ISO 26262 & IEC 61508 functional safety standards
- Small footprint solutions up to SIL 3 (design target)
- Two separate Spartan UltraScale+ devices form traditional safety architectures with redundancy

POINT-OF-CARE MEDICAL SYSTEMS

- Portable x-ray systems, hand-held diagnostic ultrasound, and patient monitoring devices
- Low active and standby power dissipation for long battery life
- Complex algorithms like beamforming, monitoring, image acquisition, and image processing benefit from resources like DSP, logic, RAM, and flexible I/Os

FEATURES

FEATURE	HIGHLIGHTS
I/O Scalability	• Up to 336 High-density I/Os (HDIOs) with 1.2V to 3.3V • Up to 104 High-performance I/Os (HPIOs) with 1.2V to 1.8V capability and max 2.5 Gb/s • Up to 132 XP5IOs with 1.2V to 1.5V and max 4266 Mb/s
Integrated RAM	• Block RAM with high-speed memory cascading is available in all devices • UltraRAM in select devices can reduce need for external SRAM • Ideal to stream acquired data into RAM locally
Built-in DDR Memory Controller	• Hardened memory controller for LPDDR4x and LPDDR5 • Up to 4266 Mb/s via XP5IO • Avoids using programmable logic for memory interfacing
Support for MIPI D-PHY	• Via soft IP core in Vivado™ IP catalog; no additional license required • Up to 3.2 Gb/s via new XP5IO and accommodates up to 4 MIPI channels • Allows direct connection of optical sensors without external PHY
Functional Safety Certified Design Flow	• AMD Vivado™ Design Suite is certified for development and validation of designs up to SIL 3 • Systematic Capability SC3 in programmable logic (design target) • Built-in memory controller targets SIL 2
Small Footprint Packages	• Package sizes from 10 mm x 10 mm to 35 mm x 35 mm • Seven different package types, from 361 to 1,156 pins/balls • 0.5 mm to 1.0 mm ball pitch
Works with MicroBlaze Soft Processors	• Instances of the MicroBlaze processor can be used without additional licenses • MicroBlaze V processor with RISC-V ISA without additional license • Ideal for Industrial IOT applications

NEXT STEPS

To learn more about automation with AMD FPGAs, visit our solutions websites: **www.xilinx.com/applications/industrial/machine-vision-systems.html** and **www.xilinx.com/applications/medical.html**

For more information on the AMD Cost-Optimized Portfolio, visit **www.amd.com/cost-optimized**

To contact your local AMD sales representative, visit **www.amd.com/en/forms/product-inquiry/adaptive-socs-and-fpgas.html**

ENDNOTES

1. Based on product datasheets for AMD Spartan UltraScale+ FPGAs versus Efinix, Intel, Lattice, and Microchip, as of February 2024, comparing the total I/O to logic cell ratios of comparable 28 nm and lower node size FPGAs. (SUS-11)
2. Projection is based on AMD internal analysis, as of January 2024, using a Total Power calculation (Static plus Dynamic power) based on the logic scale count of an Artix UltraScale AU7P FPGA to estimate the total power of Spartan UltraScale+ SU200P FPGA versus Artix 7 7A200T FPGA, using Xilinx Power Estimator (XPE) tool version 2023.1.2. Actual Total power interfacing may vary when products are released in market based on configuration, design, usages, and other factors. (SUS-06)
3. Projection is based on AMD labs internal analysis in January 2024, using Total Power calculation (Static plus Dynamic power) based on the difference in logic cell count of an AMD Artix™ UltraScale+ AU7P FPGA, to estimate the power of a 16 nm AMD Spartan UltraScale+ SU35P FPGA versus a 28 nm AMD Artix 7 7A35T FPGA, using Xilinx Power Estimator (XPE) tool version 2023.1.2. Actual Total Power will vary when final products are released in market, based on configuration, design, usage, and other factors. (SUS-03)
4. Device Reliability Report (UG116)

DISCLAIMERS

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