Encoders

Programmable Solutions for the Broadcast Industry
HDTV and Bandwidth

• HDTV proving popular with consumers in some regions
  – HDTV might even be legislated as “must carry” in the US
• Operators face adding channel capacity
  – Could mean rebuilding entire facility!
• Much rather use better compression techniques
  – Squeeze more down the same coax/fibre
  – Relatively inexpensive to implement
• Also concern about cost of providing high-definition capability at customer premise
  – Ship out new set-top boxes or upgrade in the field?
HD Transition & Next Gen Codecs

5.5x the amount of data!

Standard Def
640x480 4:3

High Definition
1920x1080 16:9
Video & Image Compression

- Bandwidth and storage capacity is precious!
- Compression helps get most out of available bandwidth/storage
  - Trade off between amount of data sent/stored & acceptable picture quality
- E.g. Uncompressed high-definition pictures take too much bandwidth to send down a 6MHz or 8MHz cable channel (up to 40Mbps)

<table>
<thead>
<tr>
<th>Definition</th>
<th>Lines/Frame</th>
<th>Pixels/Line</th>
<th>Aspect Ratios</th>
<th>Frame Rates</th>
</tr>
</thead>
<tbody>
<tr>
<td>High (HD)</td>
<td>1080</td>
<td>1920</td>
<td>16:9</td>
<td>23.976p, 24p, 29.97p, 29.97i, 30p, 30i</td>
</tr>
<tr>
<td>High (HD)</td>
<td>720</td>
<td>1280</td>
<td>16:9</td>
<td>23.976p, 24p, 29.97p 30p, 59.94p, 60p</td>
</tr>
<tr>
<td>Standard (SD)</td>
<td>480</td>
<td>704</td>
<td>4:3, 16:9</td>
<td>23.976p, 24p, 29.97p, 29.97i, 30p, 30i, 59.94p, 60p</td>
</tr>
<tr>
<td>Standard (SD)</td>
<td>480</td>
<td>640</td>
<td>16:9</td>
<td>23.976p, 24p, 29.97p, 29.97i, 30p, 30i, 59.94p, 60p</td>
</tr>
</tbody>
</table>

ATSC “Table III”

- 1920 x 1080 pixels @ 30 frames per second = ~1.5Gbps!
Coding the Difference

- If values don’t change between frames then no need to retransmit
- Working on picture differences (residuals) offers higher compression
- Lots of motion in frame (camera shake, panning, action shots) will result in residuals with lots of energy and increase bit rate requirements
Motion Estimation

- Estimation predicts next frame data by searching for macroblock matches and shifting data from previous picture along a calculated motion vector
- Predicted picture is compared to actual picture and any prediction errors calculated
- Residual frame data is further reduced with motion estimation therefore more zero values in DCT step and higher compression results
Reducing Energy in Residual

Video Frame N  Video Frame N+1  Motion Vectors

Residual Frame

Reduced Energy

More DCT coefficients will be at zero after quantization

Residual Frame After Motion Compensation
Spatial Redundancy

1. Scan picture using 16x16 pixel “macroblock”
2. Scan 8x8 blocks
4 luminance blocks & 2 chrominance (half resolution)
3. Determine luminance & chrominance values
4. Luminance samples shown (Chrominance done separately)

5. Convert to frequency components (DCT)
Output DCT coefficients
Picture reconstructed in decoder using calculated coefficients & these basis patterns

6. Human eye less sensitive to high frequencies
Publish DCT coefficients
Most energy in top left coeffs

7. Quantize higher frequencies with less bits (weighting)
Zero values for frequencies below perception threshold
8. Compress using zigzag scan & run length encoding (RLE)
e.g. blue data all “lost”
Further compression with Variable Length Coding (VLC)
MPEG-2 Video Encoder

Input Frame → DCT → Quantization → Encoding

- Motion Estimation
- Motion Compensation

Frame Buffer(s)

Inverse Quantization → Inverse DCT
MPEG-4 Video Encoder

Input Frame → DCT → Quantization → Entropy Coding → Multiplex

- DCT → Inverse Quantization → Inverse DCT

Motion Compensation → Frame Buffer(s) → Loop Filter

Motion Estimation → Shape Coding
History of Video Coding Standards

ISO/IEC
MPEG
MPEG-1 (1993)
MPEG-2 (H.262) (1994/95)
MPEG-4 v1 (1998/99)
MPEG-4 v2 (1999/00)
MPEG-4 v3 (2001)

ITU-T
VCEG
H.261 (1990)
H.263 (1995/96)
H.263+ (1997/98)
H.263++ (2000)

VC-1 (2003)

H.262
MPEG-2 (1994/95)

## MPEG Summary Overview

<table>
<thead>
<tr>
<th>MPEG-1</th>
<th>MPEG-4.2 Short Header</th>
<th>MPEG-2</th>
<th>MPEG-4.2</th>
<th>MPEG-4.10</th>
</tr>
</thead>
<tbody>
<tr>
<td>352x240</td>
<td>Sub-QCIF to 'Studio' (4k x 4k)</td>
<td>352x288 to 1920x1152</td>
<td>Sub-QCIF to 'Studio' (4k x 4k)</td>
<td>Sub-QCIF to 'Studio' (4k x 4k)</td>
</tr>
<tr>
<td>1.5Mbps</td>
<td>16kbps to 1.8Gbps</td>
<td>1.5Mbps to 40Mbps</td>
<td>16kbps to 1.8Gbps</td>
<td>64kbps to 240Mbps</td>
</tr>
<tr>
<td>Video CD MP3 (MPEG-1 Layer III)</td>
<td>Video Conferencing Internet Video 3G Mobiles/PDAs Surveillance Telemedicine</td>
<td>DVD Broadcast TV Set Top Boxes</td>
<td>Video Conferencing Internet Video 3G Mobiles/PDAs Surveillance Telemedicine</td>
<td>Video Conferencing Internet Video &amp; 3G HD-DVD Broadcast TV Set Top Boxes</td>
</tr>
</tbody>
</table>

Increasing Complexity, Improving Compression Ratio, More FPGA Resources
Codec Applications

- **Video Phones**
  - Xilinx Solution
  - Peripherals (IrDA, UART, I2C, SPI)
  - Memory Interfaces (SRAM, SDRAM, Flash)

- **Internet Video Streaming Apps**
  - Xilinx Solution
  - Partial MPEG H/W acceleration
  - Peripherals (IrDA, UART, I2C, SPI)
  - Memory Interfaces (SRAM, SDRAM, Flash)

- **Broadcast**
  - Xilinx Solution
  - Full/Partial H/W acceleration
  - High performance parallel DSP algorithms
  - Multiple processor instantiations (PPC, MicroBlaze)
  - Custom logic

- **Digital Cinema**
  - Xilinx Solution
  - Full H/W acceleration
  - Ultra High performance parallel DSP algorithms
  - Multiple processor instantiations (PPC, MicroBlaze)
  - Custom logic

Growing business for broadcast to PCs & handsets at lower rates

- **5 Kbps**
- **100 Kbps**
- **1 Mbps**
- **10 Mbps**
- **100 Mbps**
- **1 Gbps**

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**H.264 Profiles**

- **Main Profile**
  - Broadcast Applications
  - Video Conferencing, CCTV Applications

- **Extended Profile**
  - Wireless, Handheld Applications

- **Baseline Profile**
  - Video Conferencing, CCTV Applications

- **High Profile**
  - HD-DVD/Blu-Ray, Broadcast

- 8-bit 4:2:2, 10-bit 4:2:2, etc

- FREXT

- Redundant slices
- Arbitrary slice ordering
- P slices
- SI / SP slices
- Data partitioning
- B slices
- I slices

**Profiles**
- 8-bit 4:2:2, 10-bit 4:2:2, etc
FPGA/DSP Based Codecs

- **Codecs**
  - H.264
  - MPEG4
  - H.263
  - MPEG2
  - JPEG

- **Channels**
  - Few
  - Many

- **Resolution**
  - HD
  - SD
  - CIF
  - QCIF

- **Coding**
  - Encode
  - Decode
  - Simultaneous encode/decode

- **Application examples**
  - Single DSP only
  - DSP + FPGA or FPGA only

- **Few**
  - HD
  - SD
  - CIF

- **Many**
  - QCIF
Reducing Costs (& Power)

- Example savings for HD H.264 Main Profile Encoder
- Combination of FPGA and DSP also provides flexibility, familiarity & legacy support and partitioning tradeoffs too
FPGA Complements Programmable DSP

**FPGA as pre-processor**

- 148.5 MHz sample rate/pixel clock
- Examples of Pre-processing:
  - Scaling
  - De-Interlacing
  - De-noise filtering
  - Cropping

**FPGA as co-processor**

- 20.74 MHz sample rate/pixel clock
- Examples of Co-processing:
  - Motion Est.
  - CABAC
  - De-blocking
TI EVM642 and Xilinx XEVM642-2VP20
Use Familiar DSP Tools for Targeting FPGAs

Design in MATLAB Environment - Benefit from FPGA Performance - Improve Productivity
System Generator for Simulink

- Bridges gap between FPGA and DSP design flows
  - Used with Simulink/MATLAB from The MathWorks
- Automatically generates HDL/optimized algorithms
  - Shortens learning curve
  - HW redesign eliminated
  - Optimal implementation
Overloading Microprocessors

- Microprocessors excellent for sequential & control tasks
- Implementing compression algorithms can very easily overload a traditional processor
  - >50% of processor cycles may be spent evaluating one block of an algorithm (motion estimation, etc.)
  - Necessitates the need for dedicated hardware acceleration
- Processor vendors have bolted on dedicate DSP blocks for hardware acceleration
  - Inflexible and still performance limited
  - Not suitable for Studio and Digital Cinema applications
Offload Difficult Codec Blocks

• Why offload to an FPGA?
  – Saves valuable processor cycles
  – Increased quality and performance
  – Potential system cost savings
  – Ability to add more capabilities to the system

• Which portions prime targets?
  – Motion Estimation, Motion Compensation, DCT/IDCT
Traditional Processing

Math-intensive algorithms dominate the processing capacity.
FPGAs for HW/SW Integration

Offload Maths Intensive Algorithms from Embedded Processor to Fabric

Control Tasks
FIR Filter
Control Tasks
FIR Filter
Control Tasks

PowerPC Processor
OCM RAM

FIR Engine (fabric/multipliers)

PowerPC with Application-Specific Hardware Acceleration

FPGA Processing
Traditional

The Virtex-4 Advantage

Processing time
## Xilinx MPEG Solutions

### MPEG Blocks

<table>
<thead>
<tr>
<th>Block</th>
<th>Encoder</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCT</td>
<td><img src="https://www.xilinx.com/images/corporate/xilinx.png" alt="Xilinx" /></td>
<td>XAPP610</td>
</tr>
<tr>
<td>Inverse DCT</td>
<td><img src="https://www.xilinx.com/images/corporate/xilinx.png" alt="Xilinx" /></td>
<td>XAPP611</td>
</tr>
<tr>
<td>Huffman Coding</td>
<td><img src="https://www.xilinx.com/images/corporate/xilinx.png" alt="Xilinx" /></td>
<td>XAPP616</td>
</tr>
<tr>
<td>Variable Length Coding</td>
<td><img src="https://www.xilinx.com/images/corporate/xilinx.png" alt="Xilinx" /></td>
<td>XAPP621</td>
</tr>
<tr>
<td>Quantization/Inverse Coding</td>
<td><img src="https://www.xilinx.com/images/corporate/xilinx.png" alt="Xilinx" /></td>
<td>XAPP615</td>
</tr>
<tr>
<td>Huffman Decoder</td>
<td><img src="https://www.xilinx.com/images/corporate/CAST.png" alt="CAST" /></td>
<td></td>
</tr>
</tbody>
</table>

### MPEG-2

<table>
<thead>
<tr>
<th>Encoder</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPEG-2 HD Encoder</td>
<td><img src="https://www.xilinx.com/images/corporate/DumaVideo.png" alt="Duma Video" /></td>
</tr>
<tr>
<td>MPEG-2 HD Decoder</td>
<td><img src="https://www.xilinx.com/images/corporate/DumaVideo.png" alt="Duma Video" /></td>
</tr>
<tr>
<td>MPEG-2 SD Decoder</td>
<td><img src="https://www.xilinx.com/images/corporate/Conexant.png" alt="Conexant" /></td>
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</tbody>
</table>

### MPEG-4.2

<table>
<thead>
<tr>
<th>Encoder</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPEG-4.2 SP Encoder</td>
<td><img src="https://www.xilinx.com/images/corporate/xilinx.png" alt="Xilinx" /></td>
</tr>
<tr>
<td>MPEG-4.2 SP Decoder</td>
<td><img src="https://www.xilinx.com/images/corporate/xilinx.png" alt="Xilinx" /></td>
</tr>
<tr>
<td>MPEG-4.2 SH Encoder</td>
<td><img src="https://www.xilinx.com/images/corporate/4i2i.png" alt="4i2i" /></td>
</tr>
<tr>
<td>MPEG-4.2 SH Decoder</td>
<td><img src="https://www.xilinx.com/images/corporate/4i2i.png" alt="4i2i" /></td>
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<tr>
<td>MPEG-4.2 SP Encoder</td>
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</tr>
</tbody>
</table>

### H.264/AVC/MPEG-4.10

<table>
<thead>
<tr>
<th>Encoder</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>H.264 BP Encoder</td>
<td><img src="https://www.xilinx.com/images/corporate/4i2i.png" alt="4i2i" /></td>
</tr>
<tr>
<td>H.264 BP Codec</td>
<td><img src="https://www.xilinx.com/images/corporate/CAST.png" alt="CAST" /></td>
</tr>
<tr>
<td>H.264 MP Codec</td>
<td>Contact Xilinx</td>
</tr>
<tr>
<td>H.264 HP Codec</td>
<td>Contact Xilinx</td>
</tr>
</tbody>
</table>

For more info on these and our latest solutions, please check out [www.xilinx.com/ipcenter](http://www.xilinx.com/ipcenter)
H.264/AVC Encoding at IBC

## Codecs Usually Need Filters

- Most video filtering can be done using 2-D FIR filters
  - Programmability allows experimentation with different coefficients, filter windows etc to get the best picture
  - Usage examples include deblocking filters and resampling

<table>
<thead>
<tr>
<th>IP Core or Reference Design</th>
<th>Provider</th>
</tr>
</thead>
<tbody>
<tr>
<td>XAPP219 Transposed Form FIR Filters</td>
<td>Xilinx Inc.</td>
</tr>
<tr>
<td>MAC FIR</td>
<td>Xilinx Inc.</td>
</tr>
<tr>
<td>Serial Distributed Arithmetic FIR Filter</td>
<td>Xilinx Inc.</td>
</tr>
<tr>
<td>Parallel Distributed Arithmetic FIR Filter</td>
<td>Xilinx Inc.</td>
</tr>
<tr>
<td>Distributed Arithmetic FIR Filter</td>
<td>Xilinx Inc.</td>
</tr>
</tbody>
</table>

See [http://www.xilinx.com/ipcenter](http://www.xilinx.com/ipcenter) for more details
Artifact Reduction

Original uncompressed image

Compressed image with block artifacts

Reduced bandwidth/memory requirements but reduced quality

FPGA may provide deblocking filter for quality improvement
Chroma Downsampling

• Most MPEG-2 applications use 8-bit 4:2:0 sampling
• But incoming data usually 10-bit 4:2:2 video
  – Maybe via SDI (Serial Digital Interface) for example
• Conversion therefore needed before MPEG processing
  – This chroma “downsampling” is lossy form of data compression

- Xilinx FPGAs provide ideal FIR filter platform for up/downsampling
# 4:2:2 and 4:2:0 Sampling

<table>
<thead>
<tr>
<th>16x16 Macroblock</th>
<th>Luma (Y’) Samples</th>
<th>Chroma (CrCb) Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="4:2:2 Macroblock" /></td>
<td><img src="image" alt="4:2:2 Luma Samples" /></td>
<td><img src="image" alt="4:2:2 Chroma Samples" /></td>
</tr>
<tr>
<td><img src="image" alt="4:2:0 Macroblock" /></td>
<td><img src="image" alt="4:2:0 Luma Samples" /></td>
<td><img src="image" alt="4:2:0 Chroma Samples" /></td>
</tr>
</tbody>
</table>

Chroma sampling half horizontal resolution of luma

Chroma sampling half horizontal and vertical resolution of luma
Why FPGAs for Video Processing?

High Computational Workloads

256-tap Filter Example

Conventional DSP Processor - Serial

\[
\frac{1 \text{ GHz}}{256 \text{ clock cycles}} = 4 \text{ MSPS}
\]

FPGA-based DSP - Parallelism

\[
\frac{500 \text{ MHz}}{1 \text{ clock cycle}} = 500 \text{ MSPS}
\]
Statistical Multiplexing

• Awards variable bit rates to multiplexed video streams to match a fixed bandwidth allocation

• Can trade off between picture quality and bit rate
  – More complex pictures given more bits
    • e.g. motor sport (very dynamic) given much higher bit rate than a news presenter (almost static)
  – Improve overall Quality of Service (QoS)

• Squeeze more into the available bandwidth
  – Maximum number of services deliverable
    • Higher return-on-investment for broadcaster
Basic Statistical Multiplexer

Statistical Multiplexer is tightly coupled to MPEG encoders. Efficiency and performance of one will affect the other.
Xilinx in Statistical Muxes

• MPEG standards leave room for proprietary techniques to improve encoder efficiency
  – Picture quality improvements from filtering and video pre-processing (e.g. FIR, DCT in FPGA)
    • Encoding noise wastes bits

• Research new methods of bandwidth resource assignment real-time in Platform FPGA
  – e.g. New ways of gathering image impairment metrics

• Add on-chip intelligence to service prioritising with embedded microprocessor
Multiple Channels on the Platform FPGA

- Think 3D rather than 2D when designing
  - Reuse resources by multiplexing if extra horsepower available
    - e.g. If running half the max speed of FPGA, you could do twice as much in same period
  - Support multiple channels in less FPGA resources than you’d expect
SDI, HD-SDI, DVB-ASI

Free Reference Designs

XAPP247 – SDI Physical Layer Implementation
XAPP288 – SDI Video Decoder
XAPP298 – SDI Video Encoder
XAPP299 – SDI Ancillary Data and EDH Processors
XAPP509 – DVB-ASI Physical Layer Implementation
XAPP543 – 10 Gb/s Serial Digital Video Aggregation
XAPP577 – HD-SDI Integration Examples for SDV Demo Board
XAPP578 – SD-SDI Integration Example for SDV Demo Board
XAPP579 – Multi-Rate SDI Integration Examples for SDV Demo Board
XAPP580 – Reducing Size of SD-SDI EDH Processing Using PicoBlaze
XAPP625 – SDI: Video Standard Detector and Flywheel Decoder
XAPP680 – HD-SDI Transmitter Using Virtex-II Pro RocketIO MGTs
XAPP681 – HD-SDI Receiver Using Virtex-II Pro RocketIO MGTs
XAPP682 – HDTV Video Pattern Generator
XAPP683 – Multi-Rate HD/SD-SDI Transmitter Using Virtex-II Pro MGTs
XAPP684 – Multi-Rate HD/SD-SDI Receiver Using Virtex-II Pro MGTs

SDV Demo Board info and ordering
www.cook-tech.com/ctxil103.html
ML471 Virtex-4 SDAV Board

Ethernet PHY Daughter Card also available to support video-over-IP
Cost Savings Versus ASSPs

ASSP-based SDI Solution

Typical ASSP 4-channel SDI input implementation
Cost of ~$64/channel = ~$256 Total

FPGA-based SDI Solution

Xilinx 4-channel SDI input implementation
Cost of ~$13/channel = ~$52 Total

80% cheaper with an FPGA!

Approximate Standard Prices for 1K Qty
SDI, HD-SDI & ASI Solutions

• Xilinx offers unrivalled resources for FPGA-based serial video interface implementations
  – Free of charge reference designs, white papers, collateral, demo boards, technical support…
• FPGAs can significantly reduce costs versus ASSP-only designs
  – Up to 80% savings possible
• Interfaces typically take little FPGA area leaving lots of room for other video processing functions
  – Or integrate expensive components into your existing FPGA
• Xilinx solutions offer impressive performance against jitter tolerance and output jitter requirements
Video-over-IP on Virtex-4

Video In/Out
- SDI
- HD-SDI
- DVB-ASI

Multiple Channels
- SDI
- HD-SDI
- DVB-ASI

Ethernet In/Out
- 10G Ethernet
- 1G Ethernet

Shows both internal and external processor options

Hard Embedded MAC
Soft IP MAC
Cable Driver or Optic module
Cable Driver or Optic module

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### Xilinx Video-over-IP Solutions

<table>
<thead>
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<th>Customer Need</th>
<th>Xilinx Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Flexible platform</strong></td>
<td><strong>FPGA is ultimate flexible platform for bridging</strong></td>
</tr>
<tr>
<td>• No clear protocol/bridging standards</td>
<td>• Available, cost-effective solutions</td>
</tr>
<tr>
<td>• Proprietary bridge between video standards and Ethernet</td>
<td>• Standards independent upgrade path</td>
</tr>
<tr>
<td><strong>Need for high speed Ethernet support</strong></td>
<td><strong>Embedded, optimised Ethernet MACs</strong></td>
</tr>
<tr>
<td>• 1Gbps for most applications</td>
<td>• Up to four 1Gbps Ethernet MACs in V-4 FX</td>
</tr>
<tr>
<td>• 10Gbps for higher performance, multiple channels</td>
<td>• MGTs (Multi Gigabit Transceivers) support &lt;1Gbps to &gt;10Gbps</td>
</tr>
<tr>
<td><strong>Processor control</strong></td>
<td><strong>Embedded IBM PowerPC 405 Processors</strong></td>
</tr>
<tr>
<td>• Data path management in software</td>
<td>• 500MHz+ performance</td>
</tr>
<tr>
<td>• Hardware/software integration with flexible tradeoffs</td>
<td>• Tightly coupled to FPGA logic</td>
</tr>
<tr>
<td><strong>Support for traditional video/audio connectivity</strong></td>
<td><strong>Suite of reference designs and application notes</strong></td>
</tr>
<tr>
<td>• Need interfaces to Serial Digital Interface (SDI), HD-SDI</td>
<td>• SDI, HD-SDI, DVB-ASI (De)Serialisers, Standards Detectors...</td>
</tr>
<tr>
<td>• Asynchronous Serial Interface (DVB-ASI)</td>
<td>• Logic and IP available for other interfaces and networks</td>
</tr>
<tr>
<td><strong>Ability to keep control of differentiators</strong></td>
<td><strong>High performance logic, memory &amp; DSP blocks</strong></td>
</tr>
<tr>
<td>• Proprietary algorithms running on high performance platform</td>
<td>• Further integration of system requirements</td>
</tr>
<tr>
<td>• Freedom to innovate</td>
<td>• Flexible processing platform for differentiating features/performance</td>
</tr>
<tr>
<td><strong>Design support and services</strong></td>
<td><strong>Complete support infrastructure</strong></td>
</tr>
<tr>
<td>• Education on products and solutions</td>
<td>• Customer education courses, 3rd party Xpert partners</td>
</tr>
<tr>
<td>• Technical support for design issues and opportunities</td>
<td>• Web support and hotlines, design services, package pricing</td>
</tr>
</tbody>
</table>

- Xilinx Video-over-IP Solutions
Quicker time to market and reprogrammability provide the best chance of achieving full product profit potential.
FPGA-Based DSP for Video

• Unrivalled DSP Performance
  – TeraMAC/s via FPGA and Embedded Multiplier fabric for:
    • Multimedia Compression - MPEG2, MPEG4, H.264, MJPEG, JPEG2000
    • Video Processing - Integrated Line Buffers, Enhancement, Pattern Recognition, Noise Reduction, Resizing, Rotation, Scalability
    • Convergence of emerging technologies in Multimedia over IP & wireless

• For Standard Definition Pixel Rates (13.5 MHz pixels)
  • SDTV Test equipment, Broadcast test equipment, Studio effects equipment, scan rate converters, frame rate converters, MPEG-2 codecs

• For High Definition Pixel Rates or Multiple Channels of Standard Definition (74.25 MHz pixels)
  • HDTV Test equipment, Broadcast test equipment, Home Theatre projection devices, Advanced studio effects, Conversions from SDTV, MPEG-2 4:2:2 profile codecs
Xilinx Encoder Solutions

• Allow offload of complex processing to hardware
  – Leave host processor to manage the system
  – Increase system performance of ASSP based design
  – Software incapable of supporting smooth, high-quality, full-screen video streaming
    • Hardware acceleration becomes a necessity!
    • MPEG sub-blocks, filters, image quality analysis

• Support for multiple channels
  – ASSPs support one or two channels at most
  – FPGAs can support many more and decrease overall system cost
    • Lower bill of materials, easier system management

• Wide range of network interfaces supported
  – Flexibility, scalability, ease of integration
Differentiate Around Standards

- FPGA implementation enables differentiation of product
  - MPEG really only defines bitstream syntax
  - Difficult to add value to totally ASSP-based algorithms
  - Proprietary compression and/or image improvements possible whilst still conforming to standard
  - IP available for time-to-market advantage
- Virtex-4 reprogrammable platform ideal for compression research
- Hidden costs associated with ASIC development (e.g. NRE, risk) not a factor with Xilinx FPGAs
  - Results in lower overall costs for production
FPGA-based Codec Solutions

- Xilinx provides the ideal codec platform
- Single devices outperform software
  - Guaranteed frame rate and high video quality regardless of the amount of motion
- Can eliminate or shrink DSP farms
  - Lower cost and lower power
- Off-the-shelf IP and support available
- Support multiple channels
- Scale between profiles (QCIF to HD)
- Supporting new, emerging codecs and profiles
  - HDV, VC-1, AVS, H.265
- Retain control over implementation
  - Differentiate through innovative motion estimation or video filter quality

H.264 on Alpha-Data ADM-XRC-4LS Virtex-4 Board
MVI Roadmap
Multimedia, Video and Imaging

Professional Broadcast
- Broadcast Encoders
- Post production
- Transrating
- Transcoding

Consumer Apps, Video & Imaging
- Signal Processing
- Video & Image Processing
- Media Gateways

Streaming Media
- Video conferencing solutions
- Portable media systems

- Video Co-processing Kit
- Video Starter Kit SX35
- Video Codec MPEG4 SP
- Video Codec H.264 BL
- Video Codec H.264 MP
- Video Codec VC1
- Video Codec JPEG2000
- Video Codec MP1-3, AC3, AAC-HE
- Video Codec H.264 BL
- Video Codec H.264 MP
- Video Codec VC1
- Video Codec JPEG2000
- Video Codec MP1-3, AC3, AAC-HE

2005
2008
Xilinx in the Broadcast Chain

- Gamma Correction
- Codecs
- Scaling/Resampling
- Colour Space
- Network Interfacing
- Chip Interfacing
- Video Filtering
- Effects (Wipe/Key)
- Memory Control
- FEC/Modulation
- System Control

[Diagram of broadcast chain with Xilinx integration]
Real Time HD/Multichannel DSP

- Highest performance on-chip DSP blocks, multipliers and memory
- Reduce size of DSP farms
- Support real time HD processing
- Support multiple channels of SD processing through resource sharing
- Reduce cost-per-channel for FEC and modulation
Cost Effective Connectivity

- Significant cost-per-channel reductions
- Portfolio of audio/video connectivity solutions
  - SDI, HD-SDI and DVB-ASI
  - Video-over-IP
- Wide range of general telecom, datacom and backplane solutions available
  - Ethernet, PCI Express, ATM, Fibre Channel, SONET, SPI RapidIO, HyperTransport...

~70% cheaper than ASSP SDI solutions!
Flexible Embedded Processing

**PicoBlaze**
- 8-bit Microcontroller
- Simple state-machines and “localised” on-chip control
- Pixel processing & display control

**MicroBlaze PowerPC™**
- 32-bit Microprocessors
- Cost/performance tradeoffs
- Extensive peripherals, RTOS & bus structures
- Networking & wireless comms, control & instrumentation
Xilinx in Broadcast

Programmable Solutions for the Broadcast Industry

Interfaces & Connectivity  Codecs  Video & Audio Processing  Transmission & Reception  End Applications

More info on a wide range of applications and technologies

www.xilinx.com.broadcast