Non Linear Editing

Programmable Solutions for the Broadcast Industry
Non Linear Editing

• Media editing used to mean physically splicing magnetic tape together in the production suite
• This progressed to digital splicing but access to the required stored material still used tapes
  — Slow due to linear access and spooling through unneeded material
• Modern editing suites use Non Linear Editing (NLE) based on hard disk drive storage
  — Faster direct access to material on the disk
Non Linear Editing

Network Interface

Disk Storage Subsystem

Input Processing

Disk Controller

Resolution Conversion (up/down)

Output Formatting

Main System Bus

Main CPU

Frame Stores

Video Processing

- Aspect Ratio Conversion
- Compression/Decompression
- Colour Correction
- Effects (Fade/Wipe/Key)

e.g. SDI, Fibre Channel, Gb Ethernet

Network Interface

Disk Storage Subsystem

Main System Bus
Requirements & Challenges

- **Multi-format support**
  - Standard and High Definition, Aspect Ratio etc...

<table>
<thead>
<tr>
<th>Definition</th>
<th>Lines/Frame</th>
<th>Pixels/Line</th>
<th>Aspect Ratios</th>
<th>Frame Rates</th>
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<tbody>
<tr>
<td>High (HD)</td>
<td>1080</td>
<td>1920</td>
<td>16:9</td>
<td>23.976p, 24p, 29.97p, 29.97i, 30p, 30i</td>
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<tr>
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<td>1280</td>
<td>16:9</td>
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</tr>
</tbody>
</table>

- **Cost pressures**
  - Competitive pressure from high-end commodity PC products

- **Efficiency improvements**
  - Workflow management, sharing and distributing
Hardware Acceleration

• Integration of broadcast systems into PC environment (and vice versa) is becoming more common
  — Webcasting of media to PCs
  — Delivery of material via Internet
  — Storage and retrieval of material
  — Media processing using PCs special effects & graphics
• Hardware to enable acceleration of PC based processing of broadcast quality video
Multi-Format Support

- Need ability to cope with a variety of sources
  - NTSC/PAL, TV/Internet, 4:3/16:9, SD/HD etc.
- Editing possible in native formats
- Final output conversion needed
  - Aspect Ratio Conversion, 3/2 pulldown, etc.
  - Xilinx FPGAs an ideal solution
    - Real-time processing speeds
    - Programmable to support future standards and formats
Experimenting with Tradeoffs

• It would be nice to have a fully flexible device to use for video processing designs
  — Allows changing of parameters like colour depth, bit accuracy (truncation)
  — Allows exploration of new compression techniques or acceleration of existing algorithms to improve throughput
  — Supports various frame rates and resolutions
  — Implements a wide range of new or existing filters for enhancement or noise reduction
Welcome to Xilinx FPGAs

- FPGAs are a key enabling technology for digital video processing
- Allow experimentation for prototypes leading to differentiation for production
- And still enable higher level of system integration with support for:
  - video interfaces, LAN/WAN technologies, other DSP, simple glue, memory control and state machines, backplane protocols…… the list is only limited by the imagination
FIR Filters for Xilinx FPGAs

- Most audio, image and video processing can be done based around finite impulse response (FIR) filters
  - Programmability allows experimentation with different coefficients, filter windows etc to get the best quality

See www.xilinx.com/ipcenter for more details
Basic Digital Video Effects

- LUTs For Adaptive H&V Filter Coefficients
- H & V Antialias Filter
- Reverse Address Generator
- SRAM
- Output Interpolator
- Embedded CPU
- Video
- Key
- V1 Video
- V1 Key
- VBI
H & V Antialias Filter

- BRAM Line Buffers feed Vertical FIR filters which are then passed on to horizontal FIR filter
- Coefficients are fed from LUTs depending on Nyquist transformation within the image
Wipe Example

Overlay Video

Overlay Video Fill + Key during one frame of transition

Background Video
3D-DVE Filtering Example

Improperly Filtered Video and Key

Properly Filtered Video and Key

Background Video

Transformed 3D-DVE with Perspective
Video Effects FPGA Solutions

- SDTV, HDTV, Dual-Link, 2K/4K Film resolutions
- Real Time 3D Effects
  - Transforms, splits, warps
- Editing functions
  - Keyers, Mixes, Wipes, Fades, Dissolves
- 3D Cube Colour Correction
- De-interlacer, HD-SD up-down conversion
- Phong shading model & textures for 3D surfaces
- Real time image transfer over PCI Express
  - To or from graphics, disk and PC memory

Effects done in FPGA frees up valuable CPU resources

Real Time - All The Time
No Standards for Enhancement or Noise Reduction

- The list is endless, but these are a few examples of enhancement algorithms and filters:
  - Spatial Filter Unsharp Masking
  - Digital Max-Detail
  - Laplacian of Gaussian Filter
  - Adaptive Histogram Equalization
  - Adaptive Kalman Temporal Filter
  - Non-Linear Median Filter
  - Non-Linear Fuzzy Filter
  - Wavelet Decomposition

- Or you may have a better version of your own for differentiation:
  - Is there an ASSP to support your idea?
  - Will your product volumes support ASIC development?
  - Will DSPs enable real-time support?
Filter Experimentation for Best Quality of Results

+ User selectable kernels
+ Experiment to find the filter that gives the best results (on-the-fly)
+ Parameterisable filter coefficients and windows
+ No sacrifice in performance with real-time calculations possible
Asset Management

- Media is tagged with metadata for use in software databases
  - Data about the data eases searching, storage and retrieval
  - Standards emerging but still no clear way of implementing metadata
    - Advanced Authoring Format (AAF)
    - Material eXchange Format (MXF)
  - Enables tracking of all project elements from a single location
- Transferring data across network requires considerable bandwidth
  - Both in terms of network availability and host processing power
  - Often needs to be a background task so that creative work isn’t held up
- PCs typically can’t support bandwidths required so usually need dedicated processing hardware for extra horsepower
- Xilinx FPGAs offer ideal combination of hardware and software
MXF Data Flow Example

- Ethernet Packet Framer
- MXF Framer
- Custom Logic
- SDI
- DVB-ASI
- External PHY
- External PHY
- SDI
- DVB-ASI
- Custom Interface
- Ethernet MUX
- High-Speed Data
- Low-Speed Data
- Ethernet Housekeeping
- MXF Configuration Data
- Device Control
- PowerPC
## Increasing Server Performance
### Offload TCP/IP Processing

<table>
<thead>
<tr>
<th>OSI Model</th>
<th>Examples</th>
<th>Current Method</th>
<th>NEW Method</th>
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</thead>
<tbody>
<tr>
<td>Application Layer</td>
<td>Email, Web Browser</td>
<td>Host Processor</td>
<td>FPGA TCP/IP Processing</td>
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<tr>
<td>Presentation Layer</td>
<td>HTTP, DNS, POP</td>
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<tr>
<td>Session Layer</td>
<td>Session Layer</td>
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<tr>
<td>Transport Layer</td>
<td>TCP, UDP</td>
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<tr>
<td>Network Layer</td>
<td>IPv4, IPv6</td>
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<tr>
<td>Data Link Layer</td>
<td>802.3, PPP</td>
<td>Network PHY</td>
<td></td>
</tr>
<tr>
<td>Physical Layer</td>
<td>Ethernet, ADSL</td>
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</tr>
</tbody>
</table>

Free up host processor by dealing with network interactions in a Xilinx FPGA. This dedicated FPGA processing accelerates total system performance.
SDI, HD-SDI, DVB-ASI

Free Reference Designs

XAPP247 – SDI Physical Layer Implementation
XAPP288 – SDI Video Decoder
XAPP298 – SDI Video Encoder
XAPP299 – SDI Ancillary Data and EDH Processors
XAPP509 – DVB-ASI Physical Layer Implementation
XAPP543 – 10 Gb/s Serial Digital Video Aggregation
XAPP577 – HD-SDI Integration Examples for SDV Demo Board
XAPP578 – SD-SDI Integration Example for SDV Demo Board
XAPP579 – Multi-Rate SDI Integration Examples for SDV Demo Board
XAPP580 – Reducing Size of SD-SDI EDH Processing Using PicoBlaze
XAPP625 – SDI: Video Standard Detector and Flywheel Decoder
XAPP680 – HD-SDI Transmitter Using Virtex-II Pro RocketIO MGTs
XAPP681 – HD-SDI Receiver Using Virtex-II Pro RocketIO MGTs
XAPP682 – HDTV Video Pattern Generator
XAPP683 – Multi-Rate HD/SD-SDI Transmitter Using Virtex-II Pro MGTs
XAPP684 – Multi-Rate HD/SD-SDI Receiver Using Virtex-II Pro MGTs

SDV Demo Board info and ordering
www.cook-tech.com/ctxil103.html
ML471 Virtex-4 SDAV Board

Ethernet PHY Daughter Card also available to support video-over-IP
Cost Savings Versus ASSPs

**ASSP-based SDI Solution**

- Equalizer: GS9064, $36
- Deserializer: GS9060, $28

Cost of ~$64/channel = ~$256 Total

**FPGA-based SDI Solution**

- Xilinx 4-channel SDI input implementation
- XC3S500E-4, $12

Cost of ~$13/channel = ~$52 Total

80% cheaper with an FPGA!
SDI, HD-SDI & ASI Solutions

• Xilinx offers unrivalled resources for FPGA-based serial video interface implementations
  — Free of charge reference designs, white papers, collateral, demo boards, technical support…
• FPGAs can significantly reduce costs versus ASSP-only designs
  — Up to 80% savings possible
• Interfaces typically take little FPGA area leaving lots of room for other video processing functions
  — Or integrate expensive components into your existing FPGA
• Xilinx solutions offer impressive performance against jitter tolerance and output jitter requirements
Video-over-IP on Virtex-4

Video In/Out
- SDI
- HD-SDI
- DVB-ASI

Multiple Channels

Ethernet In/Out
- 10G
- 1G

Shows both internal and external processor options
Standard Def Video-over-IP

Video In/Out

- SDI
- DVB-ASI
- Multiple Channels

External Processor

- DDR Ram

Proprietary Bridge

- MicroBlaze Processor
- DDR Ram

Ethernet In/Out

- 1G Ethernet
- 1G External PHY
- Cable Driver or Optic module

1G Ethernet

Internal (MicroBlaze) or external processor options shown
# Xilinx Video-over-IP Solutions

<table>
<thead>
<tr>
<th>Customer Need</th>
<th>Xilinx Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Flexible platform</strong></td>
<td>• FPGA is ultimate flexible platform for bridging</td>
</tr>
<tr>
<td>• No clear protocol/bridging standards</td>
<td>• Available, cost-effective solutions</td>
</tr>
<tr>
<td>• Proprietary bridge between video standards and Ethernet</td>
<td>• Standards independent upgrade path</td>
</tr>
<tr>
<td><strong>Need for high speed Ethernet support</strong></td>
<td><strong>Embedded, optimised Ethernet MACs</strong></td>
</tr>
<tr>
<td>• 1Gbps for most applications</td>
<td>• Up to four 1Gbps Ethernet MACs in V-4 FX</td>
</tr>
<tr>
<td>• 10Gbps for higher performance, multiple channels</td>
<td>• MGTs (Multi Gigabit Transceivers) support &lt;1Gbps to &gt;10Gbps</td>
</tr>
<tr>
<td><strong>Processor control</strong></td>
<td><strong>Embedded IBM PowerPC 405 Processors</strong></td>
</tr>
<tr>
<td>• Data path management in software</td>
<td>• 500MHz+ performance</td>
</tr>
<tr>
<td>• Hardware/software integration with flexible tradeoffs</td>
<td>• Tightly coupled to FPGA logic</td>
</tr>
<tr>
<td><strong>Support for traditional video/audio connectivity</strong></td>
<td><strong>Suite of reference designs and application notes</strong></td>
</tr>
<tr>
<td>• Need interfaces to Serial Digital Interface (SDI), HD-SDI</td>
<td>• SDI, HD-SDI, DVB-ASI (De)Serialisers, Standards Detectors…</td>
</tr>
<tr>
<td>• Asynchronous Serial Interface (DVB-ASI)</td>
<td>• Logic and IP available for other interfaces and networks</td>
</tr>
<tr>
<td><strong>Ability to keep control of differentiators</strong></td>
<td><strong>High performance logic, memory &amp; DSP blocks</strong></td>
</tr>
<tr>
<td>• Proprietary algorithms running on high performance platform</td>
<td>• Further integration of system requirements</td>
</tr>
<tr>
<td>• Freedom to innovate</td>
<td>• Flexible processing platform for differentiating features/performance</td>
</tr>
<tr>
<td><strong>Design support and services</strong></td>
<td><strong>Complete support infrastructure</strong></td>
</tr>
<tr>
<td>• Education on products and solutions</td>
<td>• Customer education courses, 3rd party Xpert partners</td>
</tr>
<tr>
<td>• Technical support for design issues and opportunities</td>
<td>• Web support and hotlines, design services, package pricing</td>
</tr>
</tbody>
</table>
Why FPGAs for A/V Processing?

High Computational Workloads

256-tap Filter Example

Conventional DSP Processor - Serial

1 GHz
---
256 clock cycles

= 4 MSPS

FPGA-based DSP - Parallelism

500 MHz
---
1 clock cycle

= 500 MSPS
Traditional Processing

Math-intensive algorithms dominate the processing capacity

Processing time

Traditional

FIR Filter

Control Tasks

FIR Filter

Control Tasks

FIR Filter

CPU

RAM
FPGAs for HW/SW Integration

Offload Maths Intensive Algorithms from Embedded Processor to Fabric

PowerPC with Application-Specific Hardware Acceleration

The Virtex-4 Advantage

Processing time
FPGA-Based DSP for Video

• Unrivalled DSP Performance
  — TeraMAC/s via FPGA and Embedded Multiplier fabric for:
    • Multimedia Compression - MPEG2, MPEG4, H.264, MJPEG, JPEG2000
    • Video Processing - Integrated Line Buffers, Enhancement, Pattern Recognition, Noise Reduction, Resizing, Rotation, Scalability
    • Convergence of emerging technologies in Multimedia over IP & wireless

• For Standard Definition Pixel Rates (13.5 MHz pixels)
  • SDTV Test equipment, Broadcast test equipment, Studio effects equipment, scan rate converters, frame rate converters, MPEG-2 codecs

• For High Definition Pixel Rates or Multiple Channels of Standard Definition (74.25 MHz pixels)
  • HDTV Test equipment, Broadcast test equipment, Home Theatre projection devices, Advanced studio effects, Conversions from SDTV, MPEG-2 4:2:2 profile codecs
The Best of Both Worlds

- Off the shelf devices
- Faster time-to-market
- Rapid adoption of standards
- Real time prototyping

- Parallel processing
- Support high data rates
- Optimal bit widths
- No real-time software coding

Xilinx DSP Solutions Offer the Best of Both Worlds With Low Cost!
# Xilinx JPEG Solutions

## JPEG Blocks
<table>
<thead>
<tr>
<th></th>
<th>XAPP610</th>
<th>XAPP611</th>
<th>XAPP616</th>
<th>XAPP621</th>
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<tr>
<td>DCT</td>
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## Baseline JPEG
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<thead>
<tr>
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<tr>
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## Motion JPEG
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## JPEG2000
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For more info on these and our latest solutions, please check out [www.xilinx.com/ipcenter](http://www.xilinx.com/ipcenter)
### Xilinx MPEG Solutions

#### MPEG Blocks

<table>
<thead>
<tr>
<th>Block</th>
<th>Vendor</th>
<th>Part Number</th>
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<tbody>
<tr>
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<td>XAPP610</td>
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#### MPEG-4.2

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<tr>
<td>MPEG-4.2 SP Decoder</td>
<td>Xilinx</td>
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<td>MPEG-4.2 SH Encoder</td>
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<tr>
<td>MPEG-4.2 SH Decoder</td>
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#### MPEG-2

<table>
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<td>MPEG-2 HD Encoder</td>
<td>Duma Video</td>
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<tr>
<td>MPEG-2 HD Decoder</td>
<td>Duma Video</td>
</tr>
<tr>
<td>MPEG-2 SD Decoder</td>
<td>CONEXANT</td>
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</table>

#### H.264/AVC/MPEG-4.10

<table>
<thead>
<tr>
<th>Encoder/Decoder</th>
<th>Vendor</th>
</tr>
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<tbody>
<tr>
<td>H.264 BP Encoder</td>
<td>4i2i</td>
</tr>
<tr>
<td>H.264 BP Codec</td>
<td>CAST</td>
</tr>
<tr>
<td>H.264 MP Codec</td>
<td>Contact Xilinx</td>
</tr>
<tr>
<td>H.264 HP Codec</td>
<td>Contact Xilinx</td>
</tr>
</tbody>
</table>

For more info on these and our latest solutions, please check out [www.xilinx.com/ipcenter](http://www.xilinx.com/ipcenter)
Reducing Costs (& Power)

- Example savings for HD H.264 Main Profile Encoder
- Combination of FPGA and DSP also provides flexibility, familiarity & legacy support and partitioning tradeoffs too

30% Cost Saving

55% Cost Saving
Xilinx Audio & Video Solutions

• Enables the designer to add real value to his system
  – Allows for experimentation in development that leads to differentiation in production
  – Chipsets that support your exact requirements are never available!!

• Supports high definition real-time processing
  – Allows for hardware acceleration of key algorithms
  – More information down the pipe
  – Less memory requirements for off-line processing

• Allows system on a chip integration
  – More channels on less chips
  – Saves valuable board space and can reduce overall BOM cost
Xilinx Solutions for NLE

• **Multi-Format Support**
  – Real-time format conversion & image processing using hardware acceleration
  – High parallel processing power reduces buffer memory requirements
  – Programmable flexible support for new and future standards

• **Network Interconnectivity**
  – Support for a wide range of LAN/MAN/WAN interfaces and protocols
  – Connect to most industry standard backplanes for ease of system integration
  – High data throughput with 3.125Gbps serial IO
  – Transfer media without tying up creative processes

• **Cost Reduction**
  – FPGA system integration reduces BOM
  – Support multiple channels in a single device
  – High speed parallel processing in FPGAs reduces/removes DSP farms

• **Faster time-to-market and longer time-in-market**