Statistical Multiplexing/Remultiplexers

Programmable Solutions for the Broadcast Industry
Statistical Multiplexing

- Awards variable bit rates to multiplexed video streams to match a fixed bandwidth allocation
- Can trade off between picture quality and bit rate
  - More complex pictures given more bits
    - Motor sport (very dynamic) given much higher bit rate than news presenter (almost static)
  - Improve overall Quality of Service (QoS)
- Squeeze more into the available bandwidth
  - Maximum number of services deliverable
    - Higher return-on-investment for broadcaster
CBR, VBR and ABR

• Encoder historically set at Constant Bit Rate (CBR)
  – Complex scenes don’t get enough bits and artifacts appear
  – Simple scenes waste bits

• Now use Variable Bit Rate (VBR) encoding instead
  – Statistically, multiplexed video streams will rarely reach maximum scene complexity simultaneously
  – Unneeded bandwidth from simple scenes used for more complex scenes
  – Offers up to 3x efficiency

• The Available Bit Rate (ABR) is any bandwidth left over for data transmission
A Basic StatMux

- Bandwidth Used in Mux
- Bit Rate Weighting

Complexity from Encoders

MPEG Encoder

Allocated Bit Rates

Elementary Streams at Variable Bit Rates to Mux
Closed Loop System

MPEG Stream and Data Inputs

- HD Encoder
- Data Insertion
- SD Encoder
- SD Encoder
- SD Encoder

Bit Rate Analysis

Post-Processing

Multiplexer

Available Bandwidth

Standard Definition

High Definition

Data
Open Loop System

MPEG Stream and Data Inputs

- Bit Rate Analysis
- Bit Rate Analysis
- Bit Rate Analysis
- Bit Rate Analysis

SD Encoder
Data Insertion
SD Encoder
SD Encoder

Pre-Processing

HD Encoder

Multi-plexer

Available Bandwidth

Standard Definition
High Definition
Data

XILINX
Determining Bit Rates

- Complexity of current output image determined by multiplexer and fed back to encoder
- Next image uses these new optimised bit rates
- Some statmuxes determine complexity several frames before playout
  - Multiplexer can now bid for bandwidth as appropriate for additional efficiency
- Bit rates can be guaranteed to some premium services via operator control
Measuring Complexity

• How to measure complexity?
  – No standard algorithm for measurement
  – Need high performance hardware analysis
  – In the field upgrades useful for supporting improved algorithms

• Switching bit rate assignment quickly between scenes needs hardware performance
  – Losing even a single frame due to move from simple to complex scene is noticeable to viewers

*Xilinx FPGAs offer unrivalled performance, flexibility and upgradeability*
HW/SW Partition Example

- H.264 Encoder (in Hardware using FPGA Fabric)
- Bit Rate Analysis (in Software on PowerPC)
- HD-SDI and/or DVB-ASI
Reduce Overall Processing Time

PowerPC with Application-Specific Hardware Acceleration

The Virtex-4 Advantage
Why FPGAs for Video Processing?

High Computational Workloads

256-tap Filter Example

Conventional DSP Processor - Serial

- Data In
- Coefficients
- MAC Unit
- 256 loops needed to process samples
- Data Out

\[ \frac{1 \text{ GHz}}{256 \text{ clock cycles}} = 4 \text{ MSPS} \]

FPGA-based DSP - Parallelism

- Data in
- C0, C1, C2, C3, C4, C5, C6, C7, C254, C255
- Data out

\[ \frac{500 \text{ MHz}}{1 \text{ clock cycle}} = 500 \text{ MSPS} \]
Supporting Multiple Streams

• Multiple streams require multiple encoders
  – Scalability and ease of connection is key
    • Flexible network connectivity required
  – Improved system integration is attractive
    • Multiple channel support in one product
    • HD, SD and data currently require different products

• Support for new types of stream requires field upgrades
  – e.g. Use of new compression standards
Multiple Channels on the Platform FPGA

- Think 3D rather than 2D when designing
  - Reuse resources by multiplexing if extra horsepower available
    - e.g. If running half the max speed of FPGA, you could do twice as much in same period
  - Support multiple channels in less FPGA resources than you’d expect
Time-to-Market Value

Quicker time to market and reprogrammability provide the best chance of achieving full product profit potential.

- Fastest time to market
- Additional profit from field upgrades
- 1st to market profit
- Reduced profit for late introduction
- Longest time in market
FPGA-Based DSP for Video

• Unrivalled DSP Performance
  – TeraMAC/s via FPGA and Embedded Multiplier fabric for:
    • Multimedia Compression - MPEG2, MPEG4, H.264, MJPEG, JPEG2000
    • Video Processing - Integrated Line Buffers, Enhancement, Pattern Recognition, Noise Reduction, Resizing, Rotation, Scalability
    • Convergence of emerging technologies in Multimedia over IP & wireless

• For Standard Definition Pixel Rates (13.5 MHz pixels)
  • SDTV Test equipment, Broadcast test equipment, Studio effects equipment, scan rate converters, frame rate converters, MPEG-2 codecs

• For High Definition Pixel Rates or Multiple Channels of Standard Definition (74.25 MHz pixels)
  • HDTV Test equipment, Broadcast test equipment, Home Theatre projection devices, Advanced studio effects, Conversions from SDTV, MPEG-2 4:2:2 profile codecs
Xilinx in Statistical Muxes

• Research new methods of bandwidth resource assignment real-time in Platform FPGA
  – e.g. Figure out new ways of gathering image impairment metrics
• Xilinx devices offer real time analysis and encoding using calculated parameters
• Add on-chip intelligence to service prioritising with embedded microprocessors in Virtex-II Pro and Virtex-4 FPGAs
  – Flexible platforms for closely coupled hardware/software partitioning
• Codec standards leave room for proprietary techniques to improve encoder efficiency
  – Picture quality improvements from filtering and video pre-processing
  – Novel motion estimation and requantization algorithms not supported by any standard products
Differentiate Around Standards

- FPGA implementation enables differentiation of product
  - MPEG really only defines bitstream syntax
  - Difficult to add value to totally ASSP-based algorithms
  - Proprietary compression and/or image improvements possible whilst still conforming to standard
  - IP available for time-to-market advantage
- Virtex-4 reprogrammable platform ideal for compression research
- Hidden costs associated with ASIC development (e.g. NRE, risk) not a factor with Xilinx FPGAs
  - Results in lower overall costs for production
SDI, HD-SDI, DVB-ASI

**Free Reference Designs**

- XAPP247 – SDI Physical Layer Implementation
- XAPP288 – SDI Video Decoder
- XAPP298 – SDI Video Encoder
- XAPP299 – SDI Ancillary Data and EDH Processors
- XAPP509 – DVB-ASI Physical Layer Implementation
- XAPP543 – 10 Gb/s Serial Digital Video Aggregation
- XAPP577 – HD-SDI Integration Examples for SDV Demo Board
- XAPP578 – SD-SDI Integration Example for SDV Demo Board
- XAPP579 – Multi-Rate SDI Integration Examples for SDV Demo Board
- XAPP580 – Reducing Size of SD-SDI EDH Processing Using PicoBlaze
- XAPP625 – SDI: Video Standard Detector and Flywheel Decoder
- XAPP680 – HD-SDI Transmitter Using Virtex-II Pro RocketIO MGTs
- XAPP681 – HD-SDI Receiver Using Virtex-II Pro RocketIO MGTs
- XAPP682 – HDTV Video Pattern Generator
- XAPP683 – Multi-Rate HD/SD-SDI Transmitter Using Virtex-II Pro MGTs
- XAPP684 – Multi-Rate HD/SD-SDI Receiver Using Virtex-II Pro MGTs

SDV Demo Board info and ordering
www.cook-tech.com/ctxil103.html
ML471 Virtex-4 SDAV Board

Ethernet PHY Daughter Card also available to support video-over-IP
Cost Savings Versus ASSPs

ASSP-based SDI Solution

Typical ASSP 4-channel SDI input implementation
Cost of ~$64/channel = ~$256 Total

FPGA-based SDI Solution

Xilinx 4-channel SDI input implementation
Cost of ~$13/channel = ~$52 Total

Approximate Standard Prices for 1K Qty

Equalizer GS9064 $36
Deserializer GS9060 $28

$12

80% cheaper with an FPGA!
SDI, HD-SDI & ASI Solutions

- Xilinx offers unrivalled resources for FPGA-based serial video interface implementations
  - Free of charge reference designs, white papers, collateral, demo boards, technical support…
- FPGAs can significantly reduce costs versus ASSP-only designs
  - Up to 80% savings possible
- Interfaces typically take little FPGA area leaving lots of room for other video processing functions
  - Or integrate expensive components into your existing FPGA
- Xilinx solutions offer impressive performance against jitter tolerance and output jitter requirements
Video-over-IP on Virtex-4

**Video In/Out**
- SDI
- HD-SDI
- DVB-ASI

**Multiple Channels**
- Shows both internal and external processor options

**Ethernet In/Out**
- 10G Ethernet
- 1G Ethernet

**Internal Processor**
- Embedded PowerPC
- TRI EMAC
- Embedded PowerPC

**External Processor**
- DDR Ram
- Soft IP MAC
- Hard Embedded MAC

**Cable Driver or Optic Module**
- Cable Driver or Optic module

**Summary**
- Virtex-4 architecture
- Video-over-IP capabilities
- Multiple input/output options
Standard Def Video-over-IP

Video In/Out

Multiple Channels

SDI

DVB-ASI

Ethernet In/Out

1G External PHY

Cable Driver or Optic module

Internal (MicroBlaze) or external processor options shown
## Xilinx Video-over-IP Solutions

<table>
<thead>
<tr>
<th>Customer Need</th>
<th>Xilinx Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>•<strong>Flexible platform</strong></td>
<td>• <strong>FPGA is ultimate flexible platform for bridging</strong></td>
</tr>
<tr>
<td>• No clear protocol/bridging standards</td>
<td>• Available, cost-effective solutions</td>
</tr>
<tr>
<td>• Proprietary bridge between video standards and Ethernet</td>
<td>• Standards independent upgrade path</td>
</tr>
<tr>
<td>• <strong>Need for high speed Ethernet support</strong></td>
<td>• <strong>Embedded, optimised Ethernet MACs</strong></td>
</tr>
<tr>
<td>• 1Gbps for most applications</td>
<td>• Up to four 1Gbps Ethernet MACs in V-4 FX</td>
</tr>
<tr>
<td>• 10Gbps for higher performance, multiple channels</td>
<td>• MGTs (Multi Gigabit Transceivers) support &lt;1Gbps to &gt;10Gbps</td>
</tr>
<tr>
<td>• <strong>Processor control</strong></td>
<td>• <strong>Embedded IBM PowerPC 405 Processors</strong></td>
</tr>
<tr>
<td>• Data path management in software</td>
<td>• 500MHz+ performance</td>
</tr>
<tr>
<td>• Hardware/software integration with flexible tradeoffs</td>
<td>• Tightly coupled to FPGA logic</td>
</tr>
<tr>
<td>• <strong>Support for traditional video/audio connectivity</strong></td>
<td>• <strong>Suite of reference designs and application notes</strong></td>
</tr>
<tr>
<td>• Need interfaces to Serial Digital Interface (SDI), HD-SDI</td>
<td>• SDI, HD-SDI, DVB-ASI (De)Serialisers, Standards Detectors…</td>
</tr>
<tr>
<td>• Asynchronous Serial Interface (DVB-ASI)</td>
<td>• Logic and IP available for other interfaces and networks</td>
</tr>
<tr>
<td>• <strong>Ability to keep control of differentiators</strong></td>
<td>• <strong>High performance logic, memory &amp; DSP blocks</strong></td>
</tr>
<tr>
<td>• Proprietary algorithms running on high performance platform</td>
<td>• Further integration of system requirements</td>
</tr>
<tr>
<td>• Freedom to innovate</td>
<td>• Flexible processing platform for differentiating features/performance</td>
</tr>
<tr>
<td>• <strong>Design support and services</strong></td>
<td>• <strong>Complete support infrastructure</strong></td>
</tr>
<tr>
<td>• Education on products and solutions</td>
<td>• Customer education courses, 3rd party Xpert partners</td>
</tr>
<tr>
<td>• Technical support for design issues and opportunities</td>
<td>• Web support and hotlines, design services, package pricing</td>
</tr>
</tbody>
</table>
# Xilinx JPEG Solutions

<table>
<thead>
<tr>
<th>JPEG Blocks</th>
<th>Baseline JPEG</th>
<th>Motion JPEG</th>
<th>JPEG2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCT</td>
<td>JPEG Fast Codec</td>
<td>Motion JPEG Codec</td>
<td>JPEG2000 Codec</td>
</tr>
<tr>
<td>XAPP610</td>
<td>CAST</td>
<td>BARCO-</td>
<td>BARCO-</td>
</tr>
<tr>
<td>Inverse DCT</td>
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</tr>
<tr>
<td>XAPP611</td>
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<td>4i2i</td>
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<tr>
<td>Huffman Coding</td>
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<tr>
<td>XAPP616</td>
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<tr>
<td>XAPP621</td>
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<tr>
<td>Quantization/Inverse</td>
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<tr>
<td>XAPP615</td>
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# Xilinx MPEG Solutions

## MPEG Blocks

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</table>

## MPEG-4.2

<table>
<thead>
<tr>
<th>Encoder Type</th>
<th>Vendor</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPEG-4.2 SP Encoder</td>
<td>Xilinx</td>
</tr>
<tr>
<td>MPEG-4.2 SP Decoder</td>
<td>Xilinx</td>
</tr>
<tr>
<td>MPEG-4.2 SH Encoder</td>
<td>CAST</td>
</tr>
<tr>
<td>MPEG-4.2 SH Decoder</td>
<td>CAST</td>
</tr>
<tr>
<td>MPEG-4.2 SP Encoder</td>
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</table>

## MPEG-2

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<tbody>
<tr>
<td>MPEG-2 HD Encoder</td>
<td>Duma Video</td>
</tr>
<tr>
<td>MPEG-2 HD Decoder</td>
<td>Duma Video</td>
</tr>
<tr>
<td>MPEG-2 SD Decoder</td>
<td>Conexant</td>
</tr>
</tbody>
</table>

## H.264/AVC/MPEG-4.10

<table>
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<th>Vendor</th>
</tr>
</thead>
<tbody>
<tr>
<td>H.264 BP Encoder</td>
<td>CAST</td>
</tr>
<tr>
<td>H.264 BP Codec</td>
<td>CAST</td>
</tr>
<tr>
<td>H.264 MP Codec</td>
<td>Contact Xilinx</td>
</tr>
<tr>
<td>H.264 HP Codec</td>
<td>Contact Xilinx</td>
</tr>
</tbody>
</table>

For more info on these and our latest solutions, please check out [www.xilinx.com/ipcenter](http://www.xilinx.com/ipcenter)
FPGA/DSP Based Codecs

Application examples
- Single DSP only
- DSP + FPGA or FPGA only

Coding
- Encode / decode
- Simultaneous encode / decode

Resolution
- HD
- SD
- CIF
- QCIF

Channels
- Few
- Many

Codecs
- JPEG
- MPEG2
- H.263
- H.264

Xilinx

Statistical Multiplexing 27
Reducing Costs (& Power)

- Example savings for HD H.264 Main Profile Encoder
- Combination of FPGA and DSP also provides flexibility, familiarity & legacy support and partitioning tradeoffs too
FPGA-based Codec Solutions

- Xilinx provides the ideal codec platform
- Single devices outperform software
  - Guaranteed frame rate and high video quality regardless of the amount of motion
- Can eliminate or shrink DSP farms
  - Lower cost and lower power
- Off-the-shelf IP and support available
- Support multiple channels
- Scale between profiles (QCIF to HD)
- Supporting new, emerging codecs and profiles
  - HDV, VC-1, AVS, H.265
- Retain control over implementation
  - Differentiate through innovative motion estimation or video filter quality

H.264 on Alpha-Data ADM-XRC-4LS Virtex-4 Board
MVI Roadmap
Multimedia, Video and Imaging

- Professional Broadcast
  - Broadcast Encoders
  - Post production
  - Transrating
  - Transcoding

- Consumer Apps, Video & Imaging
  - Signal Processing
  - Video & Image Processing
  - Media Gateways

- Streaming Media
  - Video conferencing solutions
  - Portable media systems

- Video Co-processing Kit
- Video Starter Kit SX35
- Video Starter Kit Spartan Series
- Video-on-Demand Developer Kit
- Video / Imaging Processing Utilities
- Video CODECs MPEG2
- Video CODECs H.264 BL
- Audio CODECs MP1-3, AC3, AAC-HE
- Video CODECs VC1 JPEG2000
- Video CODECs H.264 MP
- Video CODECs MPEG4 SP

2005
2008
Xilinx StatMux Solutions

• Unbeatable combination of processor embedded in logic
  – Hardware acceleration of codec sub-blocks, filters, image quality analysis
  – Software management of traffic/prioritising and rate analysis
• Less devices required for multichannel systems
  – Lower bill of materials, easier system management
• Wide range of network interfaces supported
  – Flexibility, scalability, ease of integration
• IP available for time-to-market advantage
Xilinx in the Broadcast Chain

- Gamma Correction
- Codecs
- Scaling/Resampling
- Colour Space
- Network Interfacing
- Chip Interfacing
- Video Filtering
- Effects (Wipe/Key)
- Memory Control
- FEC/Modulation
- System Control
Real Time HD/Multichannel DSP

- Highest performance on-chip DSP blocks, multipliers and memory
- Reduce size of DSP farms
- Support real time HD processing
- Support multiple channels of SD processing through resource sharing
- Reduce cost-per-channel for FEC and modulation
Cost Effective Connectivity

- Significant cost-per-channel reductions
- Portfolio of audio/video connectivity solutions
  - SDI, HD-SDI and DVB-ASI
  - Video-over-IP
- Wide range of general telecom, datacom and backplane solutions available
  - Ethernet, PCI Express, ATM, Fibre Channel, SONET, SPI RapidIO, HyperTransport...

~70% cheaper than ASSP SDI solutions!
Flexible Embedded Processing

PicoBlaze

- 8-bit Microcontroller
- Simple state-machines and “localised” on-chip control
- Pixel processing & display control

MicroBlaze PowerPC™

- 32-bit Microprocessors
- Cost/performance tradeoffs
- Extensive peripherals, RTOS & bus structures
- Networking & wireless comms, control & instrumentation
More info on a wide range of applications and technologies

www.xilinx.com/broadcast