Up/Down/Cross Converters

Programmable Solutions for the Broadcast Industry
Decisions, Decisions?

- Multiple video and graphics standards to support
  - PAL/NTSC, MPEG, JPEG...

- Multiple resolutions to support
  - SVGA, VGA, Standard Def, High Def...

- Multiple network interfaces/protocols to support
  - SDI/HD-SDI, Gigabit Ethernet, Fibre Channel...

- Xilinx FPGAs offer total scalability and flexibility to enable support of various standards now and later
  - Hardware upgradeable in the field
Video System Challenges

A Range of Resolutions

Picture Courtesy: Snell & Wilcox
HD & Video Processing

5.5x the amount of data!

Standard Def
640x480 4:3

High Definition
1920x1080 16:9
Experimenting with Tradeoffs

• It would be nice to have a fully flexible device to use for video processing designs
  – Allows changing of parameters like colour depth, bit accuracy (truncation)
  – Allows exploration of new compression techniques or acceleration of existing algorithms to improve throughput
  – Supports various frame rates and resolutions
  – Implements a wide range of new or existing enhancement or noise reduction
Welcome to Xilinx FPGAs

- FPGAs are a key enabling technology for digital video processing
- Allow experimentation for prototypes leading to differentiation for production
- And still enable higher level of system integration with support for:
  - video interfaces, LAN/WAN technologies, other DSP, simple glue, memory control and state machines, backplane protocols…… the list is only limited by the imagination
Genlock

House Reference

NTSC Buffer & Sync Stripper

Mux & Logic

Input PLL

Clock Gen & Logic

Output PLL #1

Clock Gen & Logic

Output PLL #2

Clock Gen & Logic

Output PLL #1

HD Sync Generation

625 Sync Generation

525 Sync Generation

F1L1 Generation

Config Switches

Master Timing Signals

Input PLL

Clock Gen & Logic

Output PLL #1

Clock Gen & Logic

Output PLL #2

Clock Gen & Logic

Output PLL #1

HD Sync Generation

625 Sync Generation

525 Sync Generation

F1L1 Generation

Mux & Logic

Input PLL

Clock Gen & Logic

Output PLL #1

Clock Gen & Logic

Output PLL #2

Clock Gen & Logic

Output PLL #1

HD Sync Generation

625 Sync Generation

525 Sync Generation

F1L1 Generation
SDI, HD-SDI, DVB-ASI

Free Reference Designs

XAPP247 – SDI Physical Layer Implementation
XAPP288 – SDI Video Decoder
XAPP298 – SDI Video Encoder
XAPP299 – SDI Ancillary Data and EDH Processors
XAPP509 – DVB-ASI Physical Layer Implementation
XAPP543 – 10 Gb/s Serial Digital Video Aggregation
XAPP577 – HD-SDI Integration Examples for SDV Demo Board
XAPP578 – SD-SDI Integration Example for SDV Demo Board
XAPP579 – Multi-Rate SDI Integration Examples for SDV Demo Board
XAPP580 – Reducing Size of SD-SDI EDH Processing Using PicoBlaze
XAPP625 – SDI: Video Standard Detector and Flywheel Decoder
XAPP680 – HD-SDI Transmitter Using Virtex-II Pro RocketIO MGTs
XAPP681 – HD-SDI Receiver Using Virtex-II Pro RocketIO MGTs
XAPP682 – HDTV Video Pattern Generator
XAPP683 – Multi-Rate HD/SD-SDI Transmitter Using Virtex-II Pro MGTs
XAPP684 – Multi-Rate HD/SD-SDI Receiver Using Virtex-II Pro MGTs

SDV Demo Board info and ordering
www.cook-tech.com/ctxil103.html
ML471 Virtex-4 SDAV Board

Ethernet PHY Daughter Card also available to support video-over-IP
Cost Savings Versus ASSPs

ASSP-based SDI Solution

Typical ASSP 4-channel SDI input implementation
Cost of ~$64/channel = ~$256 Total

FPGA-based SDI Solution

Xilinx 4-channel SDI input implementation
Cost of ~$13/channel = ~$52 Total

80% cheaper with an FPGA!
SDI, HD-SDI & ASI Solutions

• Xilinx offers unrivalled resources for FPGA-based serial video interface implementations
  – Free of charge reference designs, white papers, collateral, demo boards, technical support…
• FPGAs can significantly reduce costs versus ASSP-only designs
  – Up to 80% savings possible
• Interfaces typically take little FPGA area leaving lots of room for other video processing functions
  – Or integrate expensive components into your existing FPGA
• Xilinx solutions offer impressive performance against jitter tolerance and output jitter requirements
Video-over-IP on Virtex-4

Video In/Out
- SDI
- HD-SDI
- DVB-ASI

Multiple Channels

Ethernet In/Out
- 10G Ethernet
- 1G Ethernet

SOF IP MAC

Show both internal and external processor options

Cable Driver or Optic module

Hard Embedded MAC

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Standard Def Video-over-IP

Video In/Out
- SDI
- DVB-ASI

Multiple Channels

Ethernet In/Out
- 1G Ethernet
- 1G External PHY

Internal (MicroBlaze) or external processor options shown

Up/Down Converters
# Xilinx Video-over-IP Solutions

<table>
<thead>
<tr>
<th>Customer Need</th>
<th>Xilinx Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Flexible platform</strong></td>
<td><strong>FPGA is ultimate flexible platform for bridging</strong></td>
</tr>
<tr>
<td>• No clear protocol/bridging standards</td>
<td>• Available, cost-effective solutions</td>
</tr>
<tr>
<td>• Proprietary bridge between video standards and Ethernet</td>
<td>• Standards independent upgrade path</td>
</tr>
<tr>
<td><strong>Need for high speed Ethernet support</strong></td>
<td><strong>Embedded, optimised Ethernet MACs</strong></td>
</tr>
<tr>
<td>• 1Gbps for most applications</td>
<td>• Up to four 1Gbps Ethernet MACs in V-4 FX</td>
</tr>
<tr>
<td>• 10Gbps for higher performance, multiple channels</td>
<td>• MGTs (Multi Gigabit Transceivers) support &lt;1Gbps to &gt;10Gbps</td>
</tr>
<tr>
<td><strong>Processor control</strong></td>
<td><strong>Embedded IBM PowerPC 405 Processors</strong></td>
</tr>
<tr>
<td>• Data path management in software</td>
<td>• 500MHz+ performance</td>
</tr>
<tr>
<td>• Hardware/software integration with flexible tradeoffs</td>
<td>• Tightly coupled to FPGA logic</td>
</tr>
<tr>
<td><strong>Support for traditional video/audio connectivity</strong></td>
<td><strong>Suite of reference designs and application notes</strong></td>
</tr>
<tr>
<td>• Need interfaces to Serial Digital Interface (SDI), HD-SDI</td>
<td>• SDI, HD-SDI, DVB-ASI (De)Serialisers, Standards Detectors…</td>
</tr>
<tr>
<td>• Asynchronous Serial Interface (DVB-ASI)</td>
<td>• Logic and IP available for other interfaces and networks</td>
</tr>
<tr>
<td><strong>Ability to keep control of differentiators</strong></td>
<td><strong>High performance logic, memory &amp; DSP blocks</strong></td>
</tr>
<tr>
<td>• Proprietary algorithms running on high performance platform</td>
<td>• Further integration of system requirements</td>
</tr>
<tr>
<td>• Freedom to innovate</td>
<td>• Flexible processing platform for differentiating features/performance</td>
</tr>
<tr>
<td><strong>Design support and services</strong></td>
<td><strong>Complete support infrastructure</strong></td>
</tr>
<tr>
<td>• Education on products and solutions</td>
<td>• Customer education courses, 3rd party Xpert partners</td>
</tr>
<tr>
<td>• Technical support for design issues and opportunities</td>
<td>• Web support and hotlines, design services, package pricing</td>
</tr>
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Y’CbCr to R’G’B’ Converter

- Free of charge Reference Design available
- For more details check out http://www.xilinx.com/xapp/xapp283.pdf
R’G’B’ to Y’CbCr Converter

• Free of charge Reference Design available
• For more details check out http://www.xilinx.com/xapp/xapp637.pdf
**Video Test Pattern Generators**

- Application Note XAPP248 describes how to efficiently generate video test patterns in Xilinx FPGAs
- Focuses on two video test patterns
  - SMPTE EG 1-1990 Standard Color Bars
  - SMPTE RP 178-1996 SDI Checkfield
- Two basic designs are implemented
  - Using distributed SelectRAM for ROMs
  - Using block SelectRAM for ROMs
- Variations of these basic designs are also implemented
Video Effects FPGA Solutions

- SDTV, HDTV, Dual-Link, 2K/4K Film resolutions
- Real Time 3D Effects
  - Transforms, splits, warps
- Editing functions
  - Keyers, Mixes, Wipes, Fades, Dissolves
- 3D Cube Colour Correction
- **De-interlacer, HD-SD up-down conversion**
- Phong shading model & textures for 3D surfaces
- Real time image transfer over PCI Express
  - To or from graphics, disk and PC memory

Effects done in FPGA frees up valuable CPU resources

*Real Time - All The Time*
Basic Audio Effects in FPGA

SPDIF or AES In

SPDIF or AES/EBU Receive CWda01

Serial To Parallel

CoreConnect Audio In CWda20

(Master)

SPDIF or AES In

OPB BUS

software:
Volume
Treble
Bass
Echo
Reverb

CoreConnect Audio Out CWda21

(Slave)

Parallel To Serial

(Slave)

SPDIF or AES/EBU Transmit CWda02

Courtesy: coreworks
FIR Filters for Xilinx FPGAs

- Most audio, image and video processing can be done based around finite impulse response (FIR) filters
  - Programmability allows experimentation with different coefficients, filter windows etc to get the best quality

<table>
<thead>
<tr>
<th>256 Tap FIR Filter Example</th>
<th>IP Core or Reference Design</th>
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<tbody>
<tr>
<td></td>
<td>XAPP219 Transposed Form FIR Filters</td>
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<tr>
<td></td>
<td>MAC FIR</td>
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<tr>
<td></td>
<td>Serial Distributed Arithmetic FIR Filter</td>
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<tr>
<td></td>
<td>Parallel Distributed Arithmetic FIR Filter</td>
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<tr>
<td></td>
<td>Distributed Arithmetic FIR Filter</td>
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</table>

See www.xilinx.com/ipcenter for more details
Real-Time Video Resizing

Input Image

Line 1

Line 2

Line n

Vertical FIR Filter

Horizontal FIR Filter

Resized Image

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Line Buffering

- Line Buffers feed Horizontal and Vertical FIR filters to do real-time image processing without frames store.
FIR Filters for Xilinx FPGAs

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Why FPGAs for A/V Processing?

High Computational Workloads

256-tap Filter Example

Conventional DSP Processor - Serial

- 1 GHz
- 256 clock cycles
- 4 MSPS

FPGA-based DSP - Parallelism

- 500 MHz
- 1 clock cycle
- 500 MSPS
FPGA-Based DSP for Video

- Unrivalled DSP Performance
  - TeraMAC/s via FPGA and Embedded Multiplier fabric for:
    - Multimedia Compression - MPEG2, MPEG4, H.264, MJPEG, JPEG2000
    - Video Processing - Integrated Line Buffers, Enhancement, Pattern Recognition, Noise Reduction, Resizing, Rotation, Scalability
    - Convergence of emerging technologies in Multimedia over IP & wireless

- For Standard Definition Pixel Rates (13.5 MHz pixels)
  - SDTV Test equipment, Broadcast test equipment, Studio effects equipment, scan rate converters, frame rate converters, MPEG-2 codecs

- For High Definition Pixel Rates or Multiple Channels of Standard Definition (74.25 MHz pixels)
  - HDTV Test equipment, Broadcast test equipment, Home Theatre projection devices, Advanced studio effects, Conversions from SDTV, MPEG-2 4:2:2 profile codecs
Math-intensive algorithms dominate the processing capacity.
FPGAs for HW/SW Integration

Offload Maths Intensive Algorithms from Embedded Processor to Fabric

Control Tasks
FIR Filter
Control Tasks
FIR Filter
Control Tasks
FIR Filter
Control Tasks
FIR Filter

PowerPC with Application-Specific Hardware Acceleration

FPGA Processing

Traditional

The Virtex-4 Advantage

Processing time
Xilinx Audio & Video Solutions

- **Enables the designer to add real value to his system**
  - Allows for experimentation in development that leads to differentiation in production
  - Chipsets that support your *exact* requirements are never available!!

- **Supports high definition real-time processing**
  - Allows for hardware acceleration of key algorithms
  - More information down the pipe
  - Less memory requirements for off-line processing

- **Allows system on a chip integration**
  - More channels on less chips
  - Saves valuable board space and can reduce overall BOM cost
Up/Down Converter Solutions

• Complete portfolio of IP to support SoC design
  – SDI/ASI connectivity, HD and SD real-time processing
  – Hardware and software tradeoffs whilst remaining closely coupled
  – Reduce board area and bill of materials

• Flexible and upgradeable FPGA platform for differentiation
  – New algorithms, “secret sauce” enhancements

• Scaleable platform to support more channels in less chips
  – Reduce overall cost, including hidden costs like power management
  – More channels in same rack space
Xilinx in the Broadcast Chain

Gamma Correction
Codecs
Scaling/Resampling
Colour Space
Network Interfacing
Chip Interfacing
Video Filtering
Effects (Wipe/Key)
Memory Control
FEC/Modulation
System Control

Up/Down Converters
Real Time HD/Multichannel DSP

- Highest performance on-chip DSP blocks, multipliers and memory
- Reduce size of DSP farms
- Support real time HD processing
- Support multiple channels of SD processing through resource sharing
- Reduce cost-per-channel for FEC and modulation
Cost Effective Connectivity

• Significant cost-per-channel reductions
• Portfolio of audio/video connectivity solutions
  – SDI, HD-SDI and DVB-ASI
  – Video-over-IP
• Wide range of general telecom, datacom and backplane solutions available
  – Ethernet, PCI Express, ATM, Fibre Channel, SONET, SPI RapidIO, HyperTransport...

~70% cheaper than ASSP SDI solutions!
Flexible Embedded Processing

**PicoBlaze**

- 8-bit Microcontroller
- Simple state-machines and “localised” on-chip control
- Pixel processing & display control

**MicroBlaze**

- 32-bit Microprocessors
- Cost/performance tradeoffs
- Extensive peripherals, RTOS & bus structures
- Networking & wireless comms, control & instrumentation
Xilinx in Broadcast

Programmable Solutions for the Broadcast Industry

More info on a wide range of applications and technologies

www.xilinx.com/broadcast