Digital TVs
Agenda

• Introduction and market overview
• System overview
• Xilinx value proposition for Digital TV
  – Forward Error Correction
  – MPEG
  – Memory Interface
  – IEEE-1394
  – USB 2.0
  – PCI
  – Data Encryption
  – Color Space Conversion
  – LVDS
  – Clock Generation/Distribution
• Summary
Introduction & Market Overview
The Digital Age of Consumer Electronics

Digital technology brings
- Higher accuracy
- Higher reliability
- Faster speed
- Lower power
- Lower cost
Digital Logic Spawns New Consumer Products

- **Digital TV**
  - Revolutionizing the way we watch television

- **Consumer Satellite Modems**
  - Revolutionizing high speed home Internet access

- **Desktop Video Editing**
  - Delivering video editing to the home

- **Smart Card**
  - Revolutionizing the way we purchase products

- **MP3 Players**
  - The new revolution in portable digital music
ASICS & ASSPs Cannot Meet Consumer Market Requirements

- Short Product Life Cycles
- Changing Standards
- Multiple Standards
- Rapidly Evolving Features
Convergence Is Happening!

• Invisible computing embedded within everyday devices
  – Increasing intelligence of everyday appliances

• Digital revolution
  – Infrastructure: Circuit-switched to IP-based networks
  – Analog TV to Digital TV

• Internet is ubiquitous
  – Being deployed within commercial channels
    • Business-to-Business commerce, secure transaction processing, banking

• Deregulation of global infrastructure
  – Multiple industries such as telecom, cable and utilities
Integrated Digital TV (iDTV)

• Currently need either iDTV or set-top box to receive digital television broadcasts
  – iDTV is basically a TV with an integrated set-top box
• Signals received via normal TV aerial, satellite dish or cable
  – Depends on condition and type of antenna
  – Free-to-air and pay channels available
  – Maybe xDSL?
• Connection or return channel for consumer interaction
  – e.g. POTS/ISDN/Cable
• Analog broadcasts WILL switch off at some point in time!
  – Within 10 years?
    • e.g. aiming for end 2006 in US, 2010 in UK
  – High broadcast coverage required to minimize impact on consumers
HDTV

• High Definition Television offers the consumer unprecedented broadcast picture quality and digital surround sound
• Six times the current standard broadcast resolution in U.S.!
  – i.e., there are 6 times as many pixels in the same picture space
• HDTV sets are typically large scale, wide-screen, home-cinema, entertainment centers
• Success of HDTV still dependent on attractive content provision and lowering set costs (amongst other things!)
HDTV/EDTV/SDTV

- **HDTV - High Definition TV**
  - 720p vertical scanning lines or higher
  - 1920x1080i is true HDTV
  - 16:9 aspect ratio
- **EDTV - Enhanced Definition TV**
  - 480p vertical scanning lines or higher
  - Aspect ratio not specified
- **SDTV - Standard Definition TV**
  - Digital reception but can be less than EDTV resolution
  - Aspect ratio not specified
Digital TV Display Types

- Plasma Display Panel (PDP)
- Field Emission Display (FED)
- Liquid Crystal Display (LCD)
- Cathode Ray Tube (CRT)
- Organic Light Emitting Device (OLED)
- Liquid Crystal on Silicon (LCOS)
- Digital Light Processor (DLP)
Receivers and Monitors

• DTV Receiver
  – Able to decode/process and display DTV broadcasts
  – These sets have an internal tuner circuit which allows it to receive DTV broadcast signals and display them in their standard or high-definition format

• DTV Monitor
  – Has no internal processing so it requires a set-top box or connection to a processing module
  – Is capable of displaying standard or high-definition images as required by DTV standards
Interlace/Progressive Scan

Interlace
First all odd lines scanned (1/60sec) then all even lines (1/60sec) presenting a full picture (1/30sec)

Progressive
All lines scanned in single pass presenting a full picture (1/60sec)
Aspect Ratio

• The ratio between picture width and height
• 16:9 more closely represents cinema picture formats
• Digital TV receivers must be able to cope with different ratios and automatically present a picture dependent on the display format used
• Aspect Ratio Conversion (ARC) is a common function in modern TV sets
Aspect Ratio Conversion

- HDTV Source 16:9
- Normal 4:3
- Letterbox
- Pan & Scan
- Zoom/Window
- Anamorphic
Ratios and Resolutions

- FILM 2048x1536
- SXGA 2048x1536
- SXGA 1280x1024
- XGA 1024x768
- ATSC 1280x720
- HDTV 1920x1080
- ATSC 1280x720
- NTSC 720x483
- SVGA 800x600
- VGA 640x480
- PAL 720x576

Courtesy: Snell & Wilcox
# ATSC Table III
## Scanning Formats

Table III is well known in the broadcast industry. It lists standard formats from ATSC A.53 DTV Standard. There are 36 different formats available, and it doesn’t take into account line doubling, etc.

<table>
<thead>
<tr>
<th>Definition</th>
<th>Lines/Frame</th>
<th>Pixels/Line</th>
<th>Aspect Ratios</th>
<th>Frame Rates</th>
</tr>
</thead>
<tbody>
<tr>
<td>High (HD)</td>
<td>1080</td>
<td>1920</td>
<td>16:9</td>
<td>23.976p, 24p, 29.97p, 29.97i, 30p, 30i</td>
</tr>
<tr>
<td>High (HD)</td>
<td>720</td>
<td>1280</td>
<td>16:9</td>
<td>23.976p, 24p, 29.97p, 30p, 59.94p, 60p</td>
</tr>
<tr>
<td>Standard (SD)</td>
<td>480</td>
<td>704</td>
<td>4:3, 16:9</td>
<td>23.976p, 24p, 29.97p, 29.97i, 30p, 30i, 59.94p, 60p</td>
</tr>
<tr>
<td>Standard (SD)</td>
<td>480</td>
<td>640</td>
<td>16:9</td>
<td>23.976p, 24p, 29.97p, 29.97i, 30p, 30i, 59.94p, 60p</td>
</tr>
</tbody>
</table>
Displays Driving Performance

• Take an HDTV plasma display panel example:
  – 1920x1080 resolution
  – 24-bit pixels
    • 8-bit Red, Green and Blue values
  – 30 progressive frames per second

• Bandwidth = 1920 x 1080 x 24 x 30 = 1.49Gbps
Market Overview

• Various broadcast standards
  – Support different broadcast standards worldwide
    • DVB-T, ATSC, ISDB-T, (DMB-T?)
  – MPEG-2 predominantly used as DTV compression standard

• Provides improved quality
  – Support for HDTV
  – Clearer, multi-channel sound
  – Allows broadcasters flexibility in terms of bandwidth vs. quality
Worldwide Digital TV Forecast

DTV Unit Shipments and Average Sales Price, 1998-2004

Source: IDC, 2000
Digital TV Trends

- **More Channels**
  - Increased choices
  - More specialized channels
  - Immediate feedback to broadcasters
  - Maximum use of available bandwidth

- **New Services**
  - Wide-screen
  - Interactive services
  - New text channels
  - Sophisticated on-screen program information
  - Email facilities

- **Improved Quality**
  - Support for HDTV
  - No “ghosting” or other interference effects
  - Sharper digital sound
  - Allows broadcasters flexibility in terms of bandwidth vs. quality
DTV and Consumers

• 40% of consumers have no interest in digital TV*
• Happy with the services they already have
• This portion of the market is being targeted by FTA (free-to-air) digital broadcast support
• Analog WILL switch off
• New TVs will inherently support digital services
• Plug-in modules for upgrades?
• Logos appearing to help differentiate digital TVs from analog (for those who are interested)

*Source: Zarlink Semiconductor
The Market Continues to Grow Despite Tough Times

### THE BIG PICTURE

#### STILL GOTTA HAVE IT

Despite a slumping economy, consumers are still eager to get their hands on the latest audio and video gear. And why not? It's mostly cheaper now.

<table>
<thead>
<tr>
<th>CATEGORY</th>
<th>2001 UNIT SALES</th>
<th>PERCENT CHANGE FROM 2000</th>
<th>2001 AVERAGE SELLING PRICE</th>
<th>PERCENT CHANGE FROM 2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIGITAL TELEVISION</td>
<td>325,000</td>
<td>230%</td>
<td>$2,477</td>
<td>-31%</td>
</tr>
<tr>
<td>DVD</td>
<td>3,450,000</td>
<td>94</td>
<td>205</td>
<td>-25</td>
</tr>
<tr>
<td>DIGITAL CAMERA</td>
<td>3,500,000</td>
<td>66</td>
<td>286</td>
<td>-19</td>
</tr>
<tr>
<td>MP3/DIGITAL MUSIC PLAYER</td>
<td>125,000</td>
<td>59</td>
<td>212</td>
<td>-2</td>
</tr>
<tr>
<td>HOME THEATER SYSTEM</td>
<td>425,000</td>
<td>49</td>
<td>483</td>
<td>+22</td>
</tr>
<tr>
<td>HOME CD BURNER</td>
<td>125,000</td>
<td>47</td>
<td>374</td>
<td>-20</td>
</tr>
<tr>
<td>DIGITAL CAMCORDER</td>
<td>475,000</td>
<td>43</td>
<td>808</td>
<td>-16</td>
</tr>
</tbody>
</table>

*PROJECTED Data: Industry estimates, NPD Intelect Market Tracking
F.C.C. Schedule for HDTV

1997  HDTV schedule set and spectrum assigned
2002  All commercial stations to broadcast HDTV
2003  All non-commercial stations to broadcast HDTV
2004  75% of programming to be digitally simulcast
2005  100% of programming to be digitally simulcast
2006  Analog switch off, but only if 85% of market able to receive HDTV signals
HDTV
Accelerators/Inhibitors

• Accelerators
  – Higher clarity of pictures (6 times the resolution of NTSC)
  – Better color purity
  – Better quality, multi-channel sound
  – HDTV set costs falling
  – HD production costs cheaper than film (in the long run)
  – More HD content being produced
  – Resolution of modulation scheme debates (8VSB vs. COFDM)

• Inhibitors
  – Cost of sets still too high for widespread adoption
  – Lack of consumer awareness about HDTV
  – Consumer reluctance to change to HD/digital
  – Still not enough HD content
  – Land coverage of broadcasts
  – No guarantees that standards will not change
  – Bandwidth resources may be better used for multicasting SDTV content
Digital TV System Overview
Digital TV System

- ADC
- SPDIFF Audio
- SPDIFF to I2C CODEC
- MUX
- Memory Controller
- SDRAM
- MPEG-2 Decoder
- Graphics Controller
- Color MUX
- PCI Bridge
- YUV to RGB
- DAC
- DVI (TMDS)
- Display

- CPU
- NTSC Video Decoder
- Audio Decoder
- MUX
- Audio CODEC
- Audio CODEC
- I2C to SPDIFF CODEC
- Audio CODEC

- Tuner
- VSB ALT
- MUX
- 1394 PHY
- 1394 MAC
- 1394 PHY
- 1394 MAC
- QPSK
- FEC
- QAM
- FEC
- VSB ALT
- SPDIF Audio
- SPDIF to I2C CODEC
- MUX
- Memory Controller
- SDRAM

- SAT
- QPSK
- FEC
- QAM
- FEC
- QAM
- QPSK

- Cable
- 1394 PHY
- 1394 MAC
- QPSK
- FEC
- QAM
- FEC

- Home Network
- Satellite
- Cable

- RS-232C Interface
- Parallel Interface
- Serial Interface
- Keyboard/Mouse Interface

- Programable
- uP or uC
- Mixed Signal
- Memory
- Digital

- XILINX
Xilinx Value Proposition

Digital TV / HDTV
Xilinx Solutions in iDTVs

- Multiple responsibilities within the TV
  - Bridges
    - Enabling different technologies to co-exist
  - Forward Error Correction
    - Reed-Solomon, Viterbi, De-interleaving
  - Enabling broadband local loop in digital modems
    - xDSL, cable, satellite
  - MPEG co-processing
    - DCT/IDCT acceleration
    - Picture quality enhancements allow differentiation
  - Access points
    - Interfaces to broadband and home networks
  - Encryption/Decryption
    - DES, Triple DES, AES
Front End Interface

- Not cost effective to support multiple receivers
  - Cable, terrestrial, satellite and xDSL
  - Requires multiple iDTV designs

Spartan-IIIE FPGA Allows Interface To Multiple Front Ends

Interface required to support multiple ASSPs
Choice of ASSP influenced by broadcaster features
Forward Error Correction
What Does FEC Do?

• Enables the receiver to detect and correct errors automatically without requesting retransmission
• Based on the addition of redundant parity information to the data being transmitted
• One metric of the quality of the communication link is measured in terms of Bit Error Rate (BER)
• Widely used in real-time systems for the transmission of audio and video data
DVB

- Digital Video Broadcasting organization
- Formed in September 1993
- DVB now has more than 300 members
  - Broadcasters
  - Manufacturers
  - Network operators
  - Regulatory bodies
- Mission: “The creation of a harmonious digital broadcast market for all service delivery media”
- Mainly covers Europe but also promoting in U.S. and Japan
DVB Worldwide Adoption
DVB-T (Terrestrial) FEC

- RE in
  - Mixer
  - IF bandpass filter
  - ADC
  - 2K or 8K FFT
  - Demod
  - Inner de-interleave
  - Inner error correction
  - De-interleave
  - Outer error correction

- Local oscillator
- AFC
- Pilot and TPS decode
- TPS

- Video in
  - Video decoder
  - Video ES
  - Audio decoder
  - Audio ES

- Audio in
  - Timestamp counter
  - 27MHz VCO
  - Program select
  - Demultiplexer
  - PCR
  - PSI

- Video out
- Audio out

- Video decoder
- Audio decoder

- Inner de-interleave
- Inner error correction
- De-interleave
- Outer error correction

- Reed-Solomon
- Interleaver/De-interleaver
- Viterbi

- Forward Error Correction

- XILINX
ATSC

- Advanced Television Systems Committee
- Formed in September 1982
- ATSC now has more than 200 members
- Broadcasters
- Manufacturers
- Network operators
- Regulatory bodies
- Co-ordinates television standards among different communications media focusing on digital television, interactive systems, and broadband multimedia communications. Also developing digital television implementation strategies
- Adopted by U.S., Canada, S. Korea, Taiwan and Argentina
ATSC - 8VSB (Terrestrial) FEC

RF in
Mixer 1
Local oscillator 1
Local oscillator 2
IF 1
Synchronous detector (pilot locked)
NTSC filter
Equalizer
Phase noise filter
Inner de-interleave

Trellis decode
Interleaver/De-interleaver
Main de-interleave
Outer error correction
Transport stream out
ISDB

- Integrated Service for Digital Broadcast
- Developed and adopted by Japan
- Similar to DVB
  - ISDB-T uses OFDM (Orthogonal Frequency Division Multiplex)
  - Same channel coding (FEC) - Reed Solomon and convolutional/Viterbi
- Terrestrial has some additional features
  - RF channel split into 13 segments
  - 3 different modulation schemes can be used on different segments at the same time
  - Optional time interleaver for improved mobile reception
  - 4K FFT mode available
DMB

• Digital Multimedia Broadcasting
• Jointly developed by Qinghua University in Beijing and US-based Legend Silicon
• Proposed for Chinese and Hong Kong markets
• DMB-T (terrestrial) uses TDS-OFDM
• Time domain synchronous OFDM
• Said to provide better synchronization with mobile devices
## Summary of Terrestrial Systems

<table>
<thead>
<tr>
<th>Systems</th>
<th>ATSC 8-VSB</th>
<th>DVB-T COFDM</th>
<th>ISDB-T BST-OFDM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Video</td>
<td>Main Profile Syntax of ISO/IEC 13818-2 (MPEG-2 video)</td>
<td>ISO/IEC 13818-2 (MPEG-2 Layer II Audio) and Dolby AC-3</td>
<td>ISO/IEC 13818-7 (MPEG-2 AAC audio)</td>
</tr>
<tr>
<td>Audio</td>
<td>ATSC Standard A/52 (Dolby AC-3)</td>
<td>ISO/IEC 13818-2 (MPEG-2 Layer II Audio) and Dolby AC-3</td>
<td>ISO/IEC 13818-7 (MPEG-2 AAC audio)</td>
</tr>
<tr>
<td>Outer Coding</td>
<td>R-S (207, 187, t=10)</td>
<td>RS (204, 188, t=8)</td>
<td></td>
</tr>
<tr>
<td>Inner Coding</td>
<td>Rate 2/3 trellis code</td>
<td>Punctured convolutional code: Rate 1/2, 2/3, 3/4, 5/6, 7/8 Constraint length = 7, Polynomials (octal) 171, 133</td>
<td></td>
</tr>
<tr>
<td>Inner Interleaver</td>
<td>12 to 1 trellis code interleaver</td>
<td>Bitwise interleaving and frequency interleaving</td>
<td>Bitwise interleaving, frequency interleaving and selectable time interleaving</td>
</tr>
<tr>
<td>Data Randomization</td>
<td>16-bit PRBS</td>
<td>16-bit PRBS</td>
<td>16-bit PRBS</td>
</tr>
<tr>
<td>Modulation</td>
<td>8-VSB</td>
<td>COFDM QSPK, 16QAM, 64QAM Hierarchical modulation: multi resolution constellation (16QAM and 64QAM) Guard interval: 1/32, 1/16, 1/8 and 1/4 of OFDM symbol 2 modes: 2K &amp; 8K FFT</td>
<td>BST-OFDM with 13 frequency segments DQPSK, QPSK, 16QAM, 64QAM Heirarchical modulation: three different modulations on 13 segments Guard Interval: 1/32, 1/16, 1/8 and 1/4 of OFDM symbol 3 modes: 2K, 4K and 8K FFT</td>
</tr>
</tbody>
</table>
Reed-Solomon Encoder / Decoder

• Reed-Solomon
  – An error-correcting coding system that corrects multiple errors, especially burst-type errors in communication systems
  – Transmitter (encoder)
    • Data is encoded to be corrected in an event it acquires errors
  – Receiver (decoder)
    • Uses the appended encoded bits to determine errors
    • Corrects the errors upon reception of the transmitted signal
Reed-Solomon Decoder Block Diagram for iDTV
Reed-Solomon GUls

- Parameterizable encoder and decoder cores available from Xilinx
- Simply select DVB/ATSC from the Code Specification menu
- Reed-Solomon tutorials online at Xilinx IP Center
## Reed-Solomon Decoder: DVT Examples

<table>
<thead>
<tr>
<th>Features</th>
<th>ATSC 1</th>
<th>ATSC 2</th>
<th>ATSC 3</th>
<th>ATSC 4</th>
<th>DVB 1</th>
<th>DVB 2</th>
<th>DVB 3</th>
<th>DVB 4</th>
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<tbody>
<tr>
<td>Generator Start</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>k</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>n</td>
<td>187</td>
<td>187</td>
<td>187</td>
<td>187</td>
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<td>Polynomial</td>
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<td>207</td>
<td>204</td>
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<tr>
<td>Symbol Width</td>
<td>8</td>
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<td>8</td>
<td>8</td>
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<tr>
<td>Sync Mode</td>
<td>Start Pulse</td>
<td>Start Pulse</td>
<td>Start Pulse</td>
<td>Start Pulse</td>
<td>Start Pulse</td>
<td>Start Pulse</td>
<td>Start Pulse</td>
<td>Start Pulse</td>
</tr>
<tr>
<td>Clock Enable</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Synchronous Reset</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Delayed Original Data</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Erasure Decoding</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Clock Periods Per Symbol</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Memory Style</td>
<td>Automatic</td>
<td>Automatic</td>
<td>Automatic</td>
<td>Automatic</td>
<td>Automatic</td>
<td>Automatic</td>
<td>Automatic</td>
<td>Automatic</td>
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<tr>
<td>Processing Delay</td>
<td>257</td>
<td>257</td>
<td>257</td>
<td>257</td>
<td>204</td>
<td>204</td>
<td>204</td>
<td>357</td>
</tr>
<tr>
<td>Latency</td>
<td>507</td>
<td>507</td>
<td>507</td>
<td>507</td>
<td>414</td>
<td>414</td>
<td>414</td>
<td>567</td>
</tr>
<tr>
<td>Area (Slices)</td>
<td>754</td>
<td>785</td>
<td>785</td>
<td>785</td>
<td>619</td>
<td>646</td>
<td>646</td>
<td>1476</td>
</tr>
<tr>
<td>Slices Remaining</td>
<td>782</td>
<td>751</td>
<td>751</td>
<td>1279</td>
<td>917</td>
<td>890</td>
<td>890</td>
<td>1596</td>
</tr>
<tr>
<td>Maximum Clock Frequency</td>
<td>100 MHz</td>
<td>98 MHz</td>
<td>100 MHz</td>
<td>87 MHz</td>
<td>98 MHz</td>
<td>98 MHz</td>
<td>92 MHz</td>
<td>89 MHz</td>
</tr>
</tbody>
</table>
Reed-Solomon IP Solutions - Advantages

• The Xilinx decoder core is half the size of any competitor’s offering
• Automatically configured from user parameters
  – Supports all major coding standards and custom implementations
• Can be optimized for area or speed
• Incorporates Xilinx Smart-IP technology for design predictability
Viterbi

- Viterbi algorithm
  - It is a convolutional code to correct random errors
  - It minimizes the number of sequences in the trellis search as new data is received by the demodulator
  - Developed by Dr. Andrew J. Viterbi
    - Co-founder, Retired Vice chairman, Board of Directors of QUALCOMM
Viterbi Decoder Block Diagram
Viterbi Decoder IP

- Decoder of convolutional codes
- Customized VHDL source code available, allowing generation of different netlist versions
- Customized testbench for pre- and post-synthesis verification supplied with the module
Viterbi LogiCore GUI

- Fully parameterizable - includes parallel, serial & puncturing options
- Order DO-DI-VITERBI
- More info at
- http://www.xilinx.com/ipcenter
Spartan FPGA Based Viterbi Decoder

<table>
<thead>
<tr>
<th>Product Families Supported</th>
<th>Spartan, Spartan-II, Virtex, Virtex-E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Tested</td>
<td>XC2S50-6</td>
</tr>
<tr>
<td>CLBs</td>
<td>495</td>
</tr>
<tr>
<td>Clock IOBs</td>
<td>1</td>
</tr>
<tr>
<td>IOBs</td>
<td>34</td>
</tr>
<tr>
<td>Performance (MHz)</td>
<td>56</td>
</tr>
<tr>
<td>Special Features</td>
<td>4 BlockRAMs</td>
</tr>
</tbody>
</table>
Outer Interleaver

RS decoder can only correct a limited amount of errors per packet:

Interleaving spreads burst errors across several packets:
DVB Outer Interleaver

- Previous interleaver example was actually block based whereas DVB version is convolutional (Forney algorithm)
- Error dispersion idea is basically the same

[Diagram showing interleaver process with 12 locations (0 to 11) and 11 blue blocks representing 17 byte FIFOs. Arrows indicate switches to next FIFO bank after each byte, and a note indicates synch to input switch.]
Convolutional Interleaver

- Data is effectively sheared in a DVB interleaver:

This has the advantage of needing less memory for implementation
Xilinx
Interleaver/Deinterleaver GUI
## Interleaver/Deinterleaver

### iDTV Example

<table>
<thead>
<tr>
<th>Options</th>
<th>DVB 1</th>
<th>DVB 2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mode</strong></td>
<td>Interleaver</td>
<td>De-interleaver</td>
</tr>
<tr>
<td><strong>Number of Branches</strong></td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td><strong>Branch Length Constant</strong></td>
<td>17</td>
<td>17</td>
</tr>
<tr>
<td><strong>Symbol Width</strong></td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td><strong>Pipelining</strong></td>
<td>Maximum</td>
<td>Maximum</td>
</tr>
<tr>
<td><strong>Optional Pins</strong></td>
<td>FDO, RDY, RFFD</td>
<td>FDO, RDY, RFFD</td>
</tr>
<tr>
<td><strong>Memory Style</strong></td>
<td>Automatic</td>
<td>Automatic</td>
</tr>
<tr>
<td><strong>Create RPM</strong></td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><strong>Xilinx Device</strong></td>
<td>XC2V40-5</td>
<td>XC2V40-5</td>
</tr>
<tr>
<td><strong>Use IOB Flip-Flops</strong></td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><strong>Area (slices)</strong></td>
<td>79</td>
<td>110</td>
</tr>
<tr>
<td><strong>Number of Block RAMs</strong></td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td><strong>Maximum Clock Frequency</strong></td>
<td>187 MHz</td>
<td>183 MHz</td>
</tr>
</tbody>
</table>
FEC Summary

• Range of parameterizable cores available
  – Reed Solomon encoder/decoder
  – Convolutional encoder
  – Viterbi decoder
  – Interleaver/deinterleaver
  – Turbo codecs

• Intuitive generator GUI enables fast core production

• Tutorials and core details available at...

http://www.xilinx.com/ipcenter/fec_index.html
MPEG
The MPEG Algorithm

- The MPEG Encoder is composed of a number of discrete algorithmic sections:
  - Temporal Processing
    - Seeking out and removing temporal redundancy
      - Involves storing several successive images and performing motion estimation, compensation and simple algorithmic processing to derive a pixel-by-pixel difference signal
  - Spatial Processing
    - Uses DCT to remove the high frequencies not discernable by the human eye.
  - Statistical or Variable Length Encoding (VLC) to remove redundancy in the output from the DCT
DCT/IDCT Concept

- **What is DCT?**
  - Returns the discrete cosine transform of ‘video/audio input’
  - Can be referred to as the even part of the Fourier series
  - Converts an image or audio block into its equivalent frequency coefficients

- **What is IDCT?**
  - The IDCT function is the inverse of the DCT function
  - The IDCT reconstructs a sequence from its discrete cosine transform (DCT) coefficients
The image is broken into 8x8 groups, each containing 64 pixels. Three of these 8x8 groups are enlarged in this figure, showing the values of the individual pixels, a single byte value between 0 and 255.

Courtesy: The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith
Divide picture into 16 by 16 blocks. (macroblocks)

Each macroblock is 16 pixels by 16 lines. (4 blocks)

Each block is 8 pixels by 8 lines.

8 X 8 Block

DCT

Frequency Coefficients

Detailed steps in dissecting a typical digital still image prior to being DCT transformed
DCT/IDCT Compression

- Compression allows increased throughput through transmission medium
  - Video & audio compression makes multimedia systems very efficient
    - Increases CPU bandwidth
    - Higher video frame rates
    - Better audio quality
    - Enables multimedia interactivity
- DCT/IDCT are widely used in video & audio compression
Spartan-IIIE DCT/IDCT LogiCore Features

- Combined DCT/IDCT core
- Continuous one symbol per cycle processing capability
- Internal precision
  - 14 bit cosine coefficients
  - 15 bit transpose memory
- Optimized for specific Xilinx architecture
- Fully compliant with the JPEG standard (ISO/IEC10918-1)
- Supplied with Verilog and VHDL test benches
DCT/IDCT Core Overview

- 2D transform decomposed into 2 1D - operations (Stage 1 and Stage 2)
- Intermediate results stored in Transpose Memory
- Forward DCT - 8-bit unsigned input, 11-bit signed output
- Inverse DCT - 11-bit signed input, 8-bit unsigned output
- Continuous streaming - one sample per cycle processing capability

Half-Duplex Operation
Forward or Reverse, Not both simultaneously
Spartan-IIIE DCT/IDCT Solution - Performance

![Graph showing relative performance comparison between Spartan-IIIE and 266MHz 32-bit uP with Multimedia Extensions. The Spartan-IIIE shows a relative performance of 300.]
## LogiCore Implementation

<table>
<thead>
<tr>
<th>Target Device</th>
<th>Spartan-II xc2s200E-7</th>
<th>Virtex-E xcv200e-8</th>
<th>Spartan II xc2s150-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>75 MHz (est.)</td>
<td>80 MHz</td>
<td>71.4 MHz</td>
</tr>
<tr>
<td>SDTV (27 MHz)</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Time Multiplexed Channels</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HDTV (75 MHz)</td>
<td>1</td>
<td>1</td>
<td>N/A</td>
</tr>
<tr>
<td>Time Multiplexed Channels</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Size (Slices)</td>
<td>1759</td>
<td>1759</td>
<td>1728</td>
</tr>
</tbody>
</table>
Memory Controllers and Interface
Spartan-IIIE Block RAM

- True Dual-port Static RAM - 4K bits
  - Independently configurable port data width
    - 4K x 1; 2K x 2; 1K x 4; 512 x 8; 256 x 16
  - Fast synchronous read and write
    - 2.5-ns clock-to-output with 1-ns input address/data setup
Spartan-IIIE Memory Controllers

• Spartan-IIIE FPGAs
  – Unique and extensive features, flexible architecture, low cost

• Memory controller for interface to different types of SRAM, DRAM & Flash memory
  – Xilinx provides FREE VHDL source code for implementing the memory controllers in Spartan-IIIE
Memory Controller Reference Designs

- DRAM reference designs
  - 64-bit DDR DRAM controller
  - 16-bit DDR DRAM controller
  - SDRAM controller
- SRAM reference designs
  - ZBT SRAM controller
  - QDR SRAM controller
- Flash controller
  - NOR / NAND flash controller

- Embedded memory reference designs
  - CAM for ATM applications
  - CAM using shift registers
  - CAM using Block SelectRAM
  - Data-width conversion FIFO
  - 170MHz FIFO for Virtex
  - High speed FIFO for Spartan-II

These Reference Designs are Available for Immediate Download at the Memory Corner
Memory Corner

- Collaboration between Xilinx and major memory vendors to provide comprehensive web-based memory solutions
  - Free reference designs (VHDL/Verilog)
  - SRAM, DRAM & embedded FPGA memory solutions
  - Data sheets, app notes, tutorials, FAQs, design guidelines
# Bandwidth Requirements for Various Multimedia Applications

<table>
<thead>
<tr>
<th>Application</th>
<th>Technique</th>
<th>Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Video Conference Quality</td>
<td>H.261</td>
<td>0.1 Mbps</td>
</tr>
<tr>
<td>Streaming Video</td>
<td>MPEG-4</td>
<td>5Kbps - 10Mbps</td>
</tr>
<tr>
<td>VCR Quality</td>
<td>MPEG-1</td>
<td>1.2 Mbps</td>
</tr>
<tr>
<td>Broadcast Quality</td>
<td>MPEG-2</td>
<td>2 - 4 Mbps</td>
</tr>
<tr>
<td>Studio Quality Digital TV</td>
<td>ITU-R 601</td>
<td>165 Mbps</td>
</tr>
<tr>
<td>DVD/Studio Quality TV</td>
<td>MPEG-2</td>
<td>3-6 Mbps</td>
</tr>
<tr>
<td>HDTV</td>
<td>CD-DA</td>
<td>2 Gbps</td>
</tr>
<tr>
<td>HDTV</td>
<td>MPEG-2</td>
<td>25 - 34 Mbps</td>
</tr>
<tr>
<td>Streaming Audio</td>
<td>MPEG Layer 3 (MP3)</td>
<td>32 - 320 Kbps</td>
</tr>
<tr>
<td>Consumer CD-Audio</td>
<td>CD-DA</td>
<td>1441 Kbps</td>
</tr>
<tr>
<td>Consumer CD-Audio</td>
<td>MPEG with FFT</td>
<td>192 - 256 Kbps</td>
</tr>
<tr>
<td>Sound Studio Quality</td>
<td>MPEG with FFT</td>
<td>384 Kbps</td>
</tr>
<tr>
<td>Dolby AC-3</td>
<td>5.1 Channels</td>
<td>640 Kbps</td>
</tr>
<tr>
<td>Telephone (Standard)</td>
<td>G.711 PCM</td>
<td>64 Kbps</td>
</tr>
<tr>
<td>Telephone (Standard)</td>
<td>G.721 ADPCM</td>
<td>32 Kbps</td>
</tr>
<tr>
<td>Telephone (Lower)</td>
<td>GSM</td>
<td>13 Kbps</td>
</tr>
<tr>
<td>Telephone (Lower)</td>
<td>CELP</td>
<td>5 - 7 Kbps</td>
</tr>
<tr>
<td>Broadband Access (DSL)</td>
<td>ADSL</td>
<td>1.5 - 9 Mbps</td>
</tr>
<tr>
<td>Broadband Access (Cable)</td>
<td>DOCSIS</td>
<td>2 Mbps</td>
</tr>
</tbody>
</table>
IEEE-1394 & Multimedia Industry

• 1394 is the lowest cost, digital interface available for audio/video applications

• New audio/video applications are the primary market for IEEE-1394
  – Digital Television (DTV)
  – Multimedia CDROM (MMCD)
  – Home Networks

• IEEE-1394 has been accepted as the standard digital interface by the Digital VCR Conference
IEEE-1394 & Multimedia Industry

• The European Digital Video Broadcasters (DVB) have endorsed IEEE-1394 as their digital television interface
  – Several of these companies have proposed IEEE-1394 to the VESA (Video Experts Standards Association) as the digital home network media of choice

• The EIA 4.1 subcommittee has voted for IEEE-1394 as the point-to-point interface for digital TV, as well as the multi-point interface for entertainment systems

• The American National Standards Institute (ANSI) has defined Serial Bus Protocol (SBP) to encapsulate SCSI-3 for IEEE-1394
Why IEEE-1394?

• A hardware and software standard for transporting data at 100, 200, 400, or 800 megabits per second (Mbps)

• A digital interface
  – There is no need to convert digital data into analog and tolerate a loss of data integrity

• Physically small
  – The thin serial cable can replace larger and more expensive interfaces

• Inexpensive and Easy-to-use
  – There is no need for terminators, device IDs, or elaborate setup
Why IEEE-1394?

• Hot pluggable
  – Users can add or remove 1394 devices with the bus active
• Scaleable architecture
  – May mix 100, 200, and 400 Mbps devices on a bus
• Flexible topology
  – Support of daisy chaining and branching for true peer-to-peer communication
• Non-proprietary
  – There is no licensing problem to use for products

Audio/Video Digital Interface of Choice!
IEEE 1394 Protocol Stack

- **Serial Soft API**
  - Configuration & Error Control
  - Read, Write, Lock

- **Transaction Layer**
  - Packets

- **Link Layer** (Cycle control, packet transmitter, packet receiver)

- **Physical Layer** (Encode/Decode, Arbitration, Media Interface)
  - Symbols
  - Electrical Signal & Mechanical Interface

- **Serial Bus Management**

- **IEEE 1394 Physical Interface**

- **Symbols**

- **Isochronous Channels**
1394 PHY Layer

- The physical layer provides the initialization and arbitration services
  - It assures that only one node is sending data at a time
- The physical layer of the 1394 protocol includes:
  - The electrical signaling
  - The mechanical connectors and cabling
  - The arbitration mechanisms
  - The serial coding and decoding of the data being transferred or received
  - Transfer Speed detection
1394 PHY Layer

- Link Interface
  - Data
  - Control
  - LReq
  - Iso
  - Reset

- RX Decoder & Timer

- Link Arbitration & Control Logic

- Tx Encoder

- Port Interface Logic
  - PHY Clock
  - PLL
Link Layer

- Gets data packets on and off the wire
- Does error detection and correction
- Does retransmission
- Handles provision of cycle control for isochronous channels
- The link layer supplies an acknowledged datagram to the transaction layer
  - A datagram is a one-way data transfer with request confirmation
Xilinx FPGAs are ideal for implementing Link Layer Functionality
Link Controller IP - Xilinx
Enabled Differentiation
DVI Overview

- Interface to link digital graphics sources to digital displays
- One-way link supporting uncompressed HDTV signals
- Removes an unnecessary analog-digital-analog conversion step (current methods) - enables pure digital signal to display
- Based on Transition Minimized Differential Signaling (TMDS)
- Developed and promoted by the Digital Display Working Group (DDWG)
# DVI & IEEE-1394

<table>
<thead>
<tr>
<th>Stream</th>
<th>Bit Rate</th>
<th>Architecture</th>
<th>Command &amp; Control</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IEEE-1394</strong></td>
<td>Compressed MPEG-2 Transport 1394: 100, 200, or 400 Mbps, Scalable 1394b: 800 Mbps to 3.2 Gbps, Scalable</td>
<td>Peer-to-peer</td>
<td>Support for AV command &amp; control</td>
<td>Storage, networking</td>
</tr>
<tr>
<td><strong>DVI</strong></td>
<td>Uncompressed baseband Single link DVI: 4.9 Gbps Double link DVI: 9.9 Gbps</td>
<td>Point-to-point</td>
<td>No support for AV command &amp; control</td>
<td>Digital interface between a graphics chip and a monitor</td>
</tr>
</tbody>
</table>
Spartan-IIIE in Example DVI System

Image Processing / Graphics Control (e.g. Set-Top Box)

Display Driver (e.g. Plasma Display Panel)

Display Timing Control

e.g. SIL190 Tx
e.g. SIL161A Rx

TMDS DVI Link

Color Space Converter

DCT/iDCT

Graphics Controller

To video inputs & other image processing

To display panel
USB 2.0

Universal Serial Bus
USB - Universal Serial Bus

- **Low-Speed**: 1.5 Mbps
  - Mice
  - Keyboards
  - Joysticks
  - Gamepads

- **Full-Speed**: 12 Mbps
  - Modems
  - Digital Cameras
  - Printers
  - Scanners
  - Microphones
  - Legacy Conversion

- **High-Speed**: 480 Mbps
  - Mass Storage
  - Broadband
  - Home Networking
  - Residential Gateways
  - Digital Video/Audio
  - Legacy Conversion

Courtesy: Cypress Semiconductor
USB 2.0 IP Core

- Line Driver
- Serial Interface Engine (SIE)
- Clock Generator & DLLs
- SIE Control Logic Block
- Suspend Mode Control
- Parallel Interface Module (PIM)
- CPU
- DMA
- RAM
- Application Interface
- USB Controller

USB Datastream

Digital Memory Mixed Signal uP or uC Programmable IP Block
The Xilinx USB 2.0 Solution

First USB2.0 Mass Storage Reference Design
The Xilinx USB 2.0 Solution

- Kawasaki LSI, Mentor Graphics and Xilinx have partnered and developed the industry's first UTMI-compliant USB 2.0 upgradable reference design
  - Provides a USB 2.0 to SCSI technology bridge, and can be used to provide end-to-end high-bandwidth data storage
    - For hard disk drives, CD writers, DVD ROMs, etc.
  - Flexible and upgradable USB 2.0 technology bridge to multiple home networking standards
    - Such as HomePNA, HomePlug, HomeRF, IEEE-1394, IEEE802.11b
USB 2.0 Mass Storage
Reference Design Details

USB 2.0 Transceiver
Kawasaki KL5KUSB200

USB 2.0 Function Controller
Inventra MUSBHSC

2 x 1024-byte FIFOs

Microcontroller
Inventra M8051 E-Warp

Program/Data Memory
64Kbytes SRAM
64Kbytes Flash

DMA Controller

UtMI VCI

Xilinx Spartan®-II FPGA

SCSI Connector

USB 2.0 Connector
Solution - Features

- USB 2.0 Transceiver Macrocell Interface (UTMI) compliant physical layer from Kawasaki LSI
- High-speed (480Mbps) USB 2.0 functionality
- Mentor Graphics MUSBHSFC Fully Synthesizable Core Optimized for low-cost Spartan-II FPGAs
- Backward compatible with full-speed USB 1.1
- Future-proof, reprogrammable SIE
- Low-cost home networking solution
PCI - Concept

• PCI
  – Peripheral Component Interconnect
  – Originated in the PC industry
  – High performance bus that provides a processor independent data path between the CPU and high-speed peripherals
  – Robust interconnect mechanism developed to relieve the I/O bottlenecks
ASSP Replacement & Integration

System & Memory Controllers, DLLs, Level Translators ($20)

Glue Logic

External PLD
PCI Master I/F ($5)

Supported Devices
- XC2S50E
- XC2S100E
- XC2S150E
- XC2S200E
- XC2S300E

Standard Chip PCI Master I/F ($15)

Memory ($9)

*Supported Devices

PCI ASSP Replacement & Integration
PCI - A Successful Programmable Solution

- External PLD
  - 7K Gates

- External DLLs, memories, Controllers and translators

- PCI ASSP
  - PCI Master and Slave I/F

- Standard Chip

- 35K Gates Extra Logic

- XC2S50E-5 PQ208

Spartan-IIE FPGAs Lower Overall System Cost

Relative Component Cost

PCI ASSP
PCI Master and Slave I/F

The Real-PCI™
# Spartan-IIIE PCI Solutions

<table>
<thead>
<tr>
<th>Spartan-IIIE Device</th>
<th>PCI Core</th>
<th>Speed</th>
<th>Available User Logic (system gates)</th>
<th>Available BlockRAM bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>2S50E</td>
<td>PCI32</td>
<td>33 MHz 66 MHz*</td>
<td>30-35K</td>
<td>32,768</td>
</tr>
<tr>
<td>2S100E</td>
<td>PCI32</td>
<td>33 MHz 66 MHz*</td>
<td>70-75K</td>
<td>40,960</td>
</tr>
<tr>
<td>2S150E</td>
<td>PCI32</td>
<td>33 MHz 66 MHz</td>
<td>130-135K</td>
<td>49,152</td>
</tr>
<tr>
<td>2S200E</td>
<td>PCI32</td>
<td>33 MHz 66 MHz</td>
<td>180-185K</td>
<td>57,344</td>
</tr>
<tr>
<td>2S300E</td>
<td>PCI32</td>
<td>33 MHz 66 MHz</td>
<td>280-285K</td>
<td>65,536</td>
</tr>
<tr>
<td></td>
<td>PCI64</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* PCI32: 66 MHz design available using Xilinx XPERTs or Design Services
Customer Benefits

• Reduces Cost Over PCI ASSPs
  – Cost savings of more than 50%

• Integrate and Replace System Functions
  – PLL/DLL clock management devices
  – SSTL-3/HSTL translators
  – Back plane logic and drivers
  – External Memory devices
  – System & caches controllers

• Significant Time-to-Market Advantage
Data Encryption
Copy Protection and Data Encryption

• Motivation for data encryption & cryptography
  – Data privacy (integrity & secrecy)
  – Authenticating the source of the information

• Several methods of data encryption exist
  – RSA (Rivest-Shamir-Adleman), Diffie-Hellman, RC4/RC5
  – Secure Hashing Algorithm (SHA), Blowfish
  – Elliptic Curves, ElGamal, LUC (Lucas Sequence)
  – DES (Data Encryption Standard) & Triple-DES (TDES)

• Xilinx Spartan-IIE + IP Cores today provide
  – AES, DES, Triple DES, proprietary
Copy Protection Efforts

Copy-protection efforts at a glance

- CPTWG (a cross-industry forum among the movie, PC and consumer electronics industries): Five-year-old group meets regularly to propose and discuss technology issues related to DVD, including copy protection, encryption and watermarking.

- 5C (formed by Intel Corp., Hitachi Ltd., Sony Corp, Toshiba Corp. and Matsushita Electric Industrial Co.): Worked to develop Digital Transmission Content Protection (DTCP) to define a cryptographic protocol copy protection.

- 4C (initiated by Intel, IBM, Matsushita and Toshiba): Working on a Content Protection for Recordable Media and Pre-Recorded Media (CPRM/CPPM) specification that defines a renewable cryptographic method to protect entertainment content recorded on physical media.

- TCPA (formed by Compaq, HP, IBM, Intel and Microsoft): Focuses on developing a specification to deliver a set of hardware and operating-system security capabilities that customers can use to “enhance the trust and security in their computing environments,” the group said.

Courtesy: EETimes
Copy Protection
FPGAs Add Significant Value

• Security Systems Standards and Certification Act (Draft)
  – Calls for interactive digital devices to include security technologies certified by the U.S. Secretary of Commerce
• The bill becoming a law will prevent companies from shipping products without appropriate security
  – There is however no guidance on security schemes
  – A hardware based security implementation is preferred
• Lack of consensus between companies on the encryption schemes and their implementation is leading to chaos
• Copy protection for digital video products is in it’s infancy and will be a significant area of focus
Spartan-IIIE Advantages Over Hardware & Software Solutions

- High Flexibility
- Low Performance

Software Solutions

- High Performance
- Low Flexibility

Hardware Solutions

High Performance & Enhanced Security & Performance
DES Concept

• The Data Encryption Standard (DES) algorithm
  – Developed by IBM Corporation
  – Most prevalent encryption algorithm
  – Adopted by the U.S. government in 1977, as the federal standard for encryption of commercial and sensitive, yet unclassified data
  – Is a block cipher
    • Encryption algorithm that encrypts block of data all at once, and then goes on to the next block
  – Divides 64-bit plaintext into blocks of fixed length (ciphertext)
  – Enciphers using a 56-bit secret internal key
Triple-DES Concept

- Triple-DES concept
  - More powerful and more secure
  - Equivalent to performing DES 3 times on plaintext with 3 different keys
  - TDES uses 2 or 3 56-bit keys
  - With one key, TDES performs the same as DES
  - TDES implementation: serial and parallel
    - Parallel improves performance and reduces gate count
Value Proposition in DES and TDES

- High performance, many features and cost effective
- High scalability and flexibility
  - Reconfigurable fabric and Internet Reconfigurable Logic
- Embedded solutions
  - FPGA logic not used from DES/Triple-DES soft IP can be used for other IP solutions
    - DCT/IDCT and DES/TDES soft IP in a Spartan-IIIE FPGA can be used in multimedia and imaging applications
    - Increase the value proposition and reduces solution cost
- Spartan-IIIE can be programmed with broadcaster proprietary conditional access algorithms
AES (Rijndael)

• AES (Rijndael) chosen by the National Institute of Standards and Technology (NIST) as the cryptographic algorithm for use by U.S. government organizations to protect sensitive (unclassified) information
  – Rijndael block cipher named after its Dutch developers Vincent Rijmen and Joan Daemen
• Aimed to replace DES in the long run
  – DES has been successfully attacked using dedicated hardware and parallel computer networks
  – DES to be phased out
• Triple-DES expected to remain for foreseeable future
AES (Rijndael)
IP Solutions - Helion Technology

Features
- Implements AES (Rijndael) to latest NIST FIPS proposal
- 128-bit block-size, option of 128, 192 or 256-bit key-size (can be changed dynamically)
- Very fast operation – completes one AES round per master clock
- Supports data rates in excess of 10Gbps
- Separate encrypt and decrypt cores available
- Supports optional real-time roundkey generation
- All AES operating modes easily implemented (eg. ECB, CBC, OFB, CFB, MAC)
- Simple external interface
- Highly optimised for use in Xilinx FPGA technologies

Deliverables
- Target specific netlist or fully synthesisable RTL VHDL
- VHDL simulation model and testbench with FIPS test vectors
- User documentation
Spartan-IIE Encryption Solutions

- Spartan-IIE encryption solutions are NIST approved
- The programmable nature of these solutions allows easy customization based on end application requirement

<table>
<thead>
<tr>
<th>Device</th>
<th>DES</th>
<th>Triple-DES</th>
<th>AES</th>
<th>AES</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLB Slices</td>
<td>235</td>
<td>1611</td>
<td>358*</td>
<td>231**</td>
</tr>
<tr>
<td>Performance</td>
<td>94 MHz</td>
<td>48 MHz</td>
<td>82 MHz</td>
<td>82 MHz</td>
</tr>
<tr>
<td>Area Utilization</td>
<td>19.58%</td>
<td>93.22%</td>
<td>29.83%</td>
<td>19.25%</td>
</tr>
<tr>
<td>Key Size</td>
<td>56-bit</td>
<td>128-bit or two 64-bit</td>
<td>128/192/256-bit</td>
<td>128/192/256-bit</td>
</tr>
</tbody>
</table>

Note: Solution includes encryption, decryption and key generation
* 128-bit key implementation
** Key Generation offloaded to embedded μC/μP
Color Space Conversion
RGB Unity Color Space

- Mixtures of color components can be mapped into an RGB color space covering all variations from black ($0xR + 0xG + 0xB$) to white ($1xR + 1xG + 1xB$)
Spectral Response of Human Eye

• Green sensing cones in the human eye respond to most wavelengths in the light spectrum
Luminance and Color Difference

• Pictures are almost always represented as pixels on final medium
  – Whether on printed paper or TFT, PDP & CRT displays
• Pixels can be represented with 3 full bandwidth analog RGB components
  – Huge storage and transmission bandwidth requirements for high resolution, large format displays (up to 200 terabytes during post-production)
• Human eye is more receptive to brightness than it is to color
  – Full resolution of human vision is restricted to brightness variations
  – Color detail resolution is about a quarter that of brightness variations
  – Green objects will produce more stimulus than red objects of the same brightness, with blue objects producing the least
• A brightness/luma signal (Y) can be obtained by adding RGB values together which are weighted by relative eye response
Luminance and Color Difference

- ITU CCR 601 says $Y = 0.299R + 0.587G + 0.114B$
- To save bandwidth, color difference signals are sent with luma rather than RGB
- Color difference possibilities
  - R-Y
  - B-Y
  - G-Y
    As G contributes most to Y, this signal would be small and most susceptible to noise
- Simple maths can be used to reconstruct signals at the display
Color Space Converter Structure

- Fully synchronous
- Registered input and output, 1 internal pipeline stage
- Low latency (3 cycles)
- Continuous processing
- One 3-color conversion every clock cycle
- Internal 10-bit precision for accuracy
- Rounded to 8-bit outputs
Cores Available

CCIR 601 Standard

- **RGB2YCrCb**
  - \( Y = 0.257 \times R' + 0.504 \times G' + 0.098 \times B' + 16 \)
  - \( Cr = 0.439 \times R' - 0.368 \times G' - 0.071 \times B' + 128 \)
  - \( Cb = -0.148 \times R' - 0.291 \times G' + 0.439 \times B' + 128 \)
- **YCrCb2RGB**
  - \( R' = 1.164 \times (Y - 16) + 1.596 \times (Cr - 128) \)
  - \( G' = 1.164 \times (Y - 16) - 0.813 \times (Cr - 128) - 0.392 \times (Cb - 128) \)
  - \( B' = 1.164 \times (Y - 16) + 2.017 \times (Cb - 128) \)
- **RGB2YUV**
  - \( Y = 0.299 \times R' + 0.587 \times G' + 0.114 \times B' \)
  - \( U = -0.147 \times R' - 0.289 \times G' + 0.436 \times B' \)
  - \( V = 0.615 \times R' - 0.515 \times G' - 0.100 \times B' \)
- **YUV2RGB**
  - \( R' = Y + 1.140 \times V \)
  - \( G' = Y - 0.394 \times U - 0.581 \times V \)
  - \( B' = Y - 2.032 \times U \)
## Xilinx Color Space LogiCore Solutions

<table>
<thead>
<tr>
<th>Product/Cores</th>
<th>YCrCb2RGB</th>
<th>RGB2YCrCb</th>
<th>YUV2RGB</th>
<th>RGB2YUV</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Size:</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Virtex / Virtex-E</td>
<td>194 Slices</td>
<td>217 Slices</td>
<td>158 Slices</td>
<td>245 Slices</td>
</tr>
<tr>
<td><strong>Synchronous</strong></td>
<td>Full</td>
<td>Full</td>
<td>Full</td>
<td>Full</td>
</tr>
<tr>
<td><strong>Supported Family</strong></td>
<td>Spartan</td>
<td>Spartan-II</td>
<td>Spartan</td>
<td>Spartan-II</td>
</tr>
<tr>
<td></td>
<td>Spartan-II</td>
<td>Spartan-II</td>
<td>Spartan-II</td>
<td>Spartan-II</td>
</tr>
<tr>
<td></td>
<td>Spartan-IE</td>
<td>Virtex</td>
<td>Virtex</td>
<td>Virtex</td>
</tr>
<tr>
<td></td>
<td>Virtex-E</td>
<td>Virtex-E</td>
<td>Virtex-E</td>
<td>Virtex-E</td>
</tr>
<tr>
<td><strong>Latency</strong></td>
<td>3 Clock Cycles</td>
<td>3 Clock Cycles</td>
<td>3 Clock Cycles</td>
<td>3 Clock Cycles</td>
</tr>
<tr>
<td><strong>Performance:</strong></td>
<td>&gt;95 MHz</td>
<td>&gt;90 MHz</td>
<td>&gt;90 MHz</td>
<td>&gt;110 MHz</td>
</tr>
<tr>
<td>Spartan-IIE</td>
<td>&gt;95 MHz</td>
<td>&gt;90 MHz</td>
<td>&gt;90 MHz</td>
<td>&gt;110 MHz</td>
</tr>
<tr>
<td><strong>SDTV (27 MHz)</strong></td>
<td>7 (Spartan-II)</td>
<td>3 (Spartan-II)</td>
<td>8 (Spartan-II)</td>
<td>3 (Spartan-II)</td>
</tr>
<tr>
<td><strong>Time Multiplexed Channels</strong></td>
<td>7 (Spartan-II)</td>
<td>3 (Spartan-II)</td>
<td>8 (Spartan-II)</td>
<td>3 (Spartan-II)</td>
</tr>
<tr>
<td><strong>HDTV (75 MHz)</strong></td>
<td>2 (Spartan-II)</td>
<td>1 (Spartan-II)</td>
<td>3 (Spartan-II)</td>
<td>1 (Spartan-II)</td>
</tr>
<tr>
<td><strong>Time Multiplexed</strong></td>
<td>2 (Spartan-II)</td>
<td>1 (Spartan-II)</td>
<td>3 (Spartan-II)</td>
<td>1 (Spartan-II)</td>
</tr>
<tr>
<td><strong>Cost</strong></td>
<td>$995</td>
<td>$995</td>
<td>$995</td>
<td>$995</td>
</tr>
</tbody>
</table>
Xilinx Color Space Solutions

- LogiCORE Color Space Converters provide straightforward, accurate, high-performance conversion useable in a wide range of video/image applications
- More area efficient than existing cores
- Speeds ensure operation in all TV and HDTV applications
- Available through Xilinx Coregen
Clock Generation & Distribution
Clock Generation and Distribution

- Spartan-II E DLL circuits provide full clock management solution
- Clock generation
  - Synthesizing many clocks from a single reference crystal or clock
- Clock buffering and distribution
  - Providing multiple copies of a single clock
  - SDRAM clocks
- Spread spectrum clocks for EMI reduction
  - DLL circuits allow tolerance for ±2.5% variance
Introducing the Spartan-IIIE FPGA Family
Xilinx Spartan Series FPGAs

- High Performance System Features
- Software and Cores
- Smallest Die Size
- Lowest Possible Cost
- Advanced Process Technology
- Total Cost Management
- Low Cost Plastic Packages
- Streamlined Testing
Spartan-IIE FPGAs
A Natural Fit for Digital Convergence

- Xilinx Solutions Allow Customers To Thrive in Chaos
  - FPGAs traditionally offer fast time-to-market
    - First to market, increases market share and revenue advantage
  - Xilinx Online offers reconfigurability in the field
    - Allows shipped product to support revisions to the spec
    - Enables unique opportunities to add value
    - Increases lifecycle revenue yield and hence, time-in-market
  - Enables rapid product proliferation
    - New designs can be quickly turned into derivatives
  - Superior lifecycle component logistics
  - Proven FPGA technology, software, test benches

- Spartan-IIE FPGAs Are Cost Effective!!!
Taking the Cost Down...

Cost of 150K Digital Logic Over Time

Imagine if the gas companies could do the same thing! $1.00 per gallon

Gas 1 cent per gallon!!

10,000% Reduction
Spartan-IIIE: The Total Solution

- 300K Gates
  - Distributed and Block RAM
  - Fast I/O Performance

- More Gates
- More Performance

- Feature Rich
  - DLLs
  - System I/O™ (19) LVDS/LVPECL

- Cores
  - Easy Design Flow
  - Free WebPACK SW
  - Fast, Predictable Routing

- Time-to-Market

XILINX
FPGA Application Trends

- **Glue Logic**
  - Counters
  - Adders
  - 7400 Series

- **SSI/MSI**
  - Data Path
  - Memory
  - Controllers
  - uControllers

- **LSI**
  - PCI/PCI-X
  - FEC
  - FFT/FIR Filters
  - IMA (ATM)
  - Encryption
  - MP3 Decoder

- **ASSP App.**
  - Consumer
  - Set-Top Boxes
  - Digital TV
  - Cable Modem
  - Bluetooth
  - Home Networking
  - Digital Video

- **High Volume Apps.**
  - Networking
  - xDSL Modems
  - Line Cards
  - Computers
  - Graphic Cards
  - Printers
  - Bio-Medical, Industrial

1980s
1990s
2000s

Performance & Density
Spartan-IIIE - System Integration
# Spartan-IIE Features

## Value in Digital Video

<table>
<thead>
<tr>
<th>Spartan-IIE Silicon Features</th>
<th>Value for Digital Video Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Fabric and Routing, Up to 300,000 System Gates</td>
<td>Performance in excess of 20 billion MACs/second</td>
</tr>
<tr>
<td>Delay Locked Loops (DLLs)</td>
<td>Clock multiplication and division, clock mirror, Improve I/O Perf.</td>
</tr>
<tr>
<td>SelectI/O - HSTL-I, -III, -IV</td>
<td>High-speed SRAM interface</td>
</tr>
<tr>
<td>SelectI/O - SSTL3-I, -II; SSTL2-I, -II</td>
<td>High-speed DRAM interface</td>
</tr>
<tr>
<td>SelectI/O - GTL, PCI, AGP</td>
<td>Chip-to-Backplane, Chip-to-Chip interfaces</td>
</tr>
<tr>
<td>Differential Signaling - LVDS, Bus LVDS, LVPECL</td>
<td>Bandwidth management (saving the number of pins), reduced power consumption, reduced EMI, high noise immunity</td>
</tr>
<tr>
<td>SRL-16</td>
<td>16-bit Shift Register ideal for capturing high-speed or burst-mode data and to store data in DSP applications</td>
</tr>
<tr>
<td>Distributed RAM</td>
<td>DSP Coefficients, Small FIFOs</td>
</tr>
<tr>
<td>Block RAM</td>
<td>Video Line Buffers, Cache Tag Memory, Scratch-pad Memory, Packet Buffers, Large FIFOs</td>
</tr>
</tbody>
</table>
Spartan-IIIE LVDS Solution

System Applications, Clock Distribution, Cost Management, Pin Savings, EMI Reduction
What is LVDS?

- LVDS - Low Voltage Differential Signaling
- LVDS is a differential signaling interconnect technology
  - Requires two pins per channel
- LVDS was first used as a interconnectivity technology in laptops and displays to alleviate EMI issues
- Technology is now widely used in:
  - A broad spectrum of telecom and networking applications
  - Mainstream consumer applications like digital video and displays
Differential Signaling Benefits

• Higher performance per pin pair
• Reduced EMI
  – Low output voltage swing
  – Relatively slow edge rates (dV/dt)
• High noise immunity
  – Switching noise cancels between the two lines
  – Data is not affected by the noise
    • External noise affects both lines, but the voltage difference stays about the same
• Reduced power consumption
# Spartan-IIIE Differential I/O Counts

<table>
<thead>
<tr>
<th>Device</th>
<th>TQ144</th>
<th>PQ208</th>
<th>FT256</th>
<th>FG456</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>User</td>
<td>Diff</td>
<td>User</td>
<td>Diff</td>
</tr>
<tr>
<td>XC2S50E</td>
<td>102</td>
<td>28</td>
<td>146</td>
<td>50</td>
</tr>
<tr>
<td>XC2S100E</td>
<td>102</td>
<td>28</td>
<td>146</td>
<td>50</td>
</tr>
<tr>
<td>XC2S150E</td>
<td>146</td>
<td>50</td>
<td>182</td>
<td>84</td>
</tr>
<tr>
<td>XC2S200E</td>
<td>146</td>
<td>50</td>
<td>182</td>
<td>84</td>
</tr>
<tr>
<td>XC2S300E</td>
<td>146</td>
<td>50</td>
<td>182</td>
<td>84</td>
</tr>
</tbody>
</table>

User = Maximum number of User I/Os available  
Diff = Maximum number of Differential Paired I/Os available
Spartan-IIIE LVDS Support

• All IOBs have LVDS/BLVDS/LVPECL capability
• IOBs configured as LVDS can be:
  – Synchronous or asynchronous
  – Input or output
• Two IOBs (pair) form one LVDS signal.
  – One IOB will function as + or P
  – The other IOB will function as - or N.
• LVDS pin pairs are indicated in the datasheet
• Maximum number of LVDS pin-pairs: 120
Bus LVDS and LVPECL

- **Bus LVDS** - Bi-directional LVDS
  - The device can transmit and receive LVDS signals through the same pins
  - Requires different termination than LVDS
- **LVPECL** - Low Voltage Positive Emitter Coupled Logic
  - Well known industry standard for fast clocking and interconnectivity
  - Voltage swing (~750 mV) over two differential connections
Spartan-IIIE as a Differential Driver

Capable of driving any standard LVDS or LVPECL receiver
Spartan-IIIE can be driven by any standard LVDS or LVPECL driver
Spartan-IIIE receiver complies with the LVDS or LVPECL specs
Spartan-IIIE Core Support

- On-chip memory & storage
  - Distributed, BlockRAM, FIFOs
- Bus products
  - PCI (64- & 32-bit, 33/66MHz), Arbiter, CAN bus interface
- DSP functions (FIR filter)
- Error correction
  - Reed-Solomon, Viterbi
- Encryption (DES & TDES)
- Microprocessor
  - ARC 32-bit configurable RISC, 8-bit 8051 microcontroller
- Memory controllers (10+)
  - SDRAM, QDR SRAM
- Communications
  - ATM (IMA, UTOPIA), Fast Ethernet (MAC)
- Telecom
  - CDMA matched filter, HDLC, DVB satellite, ADPCM speech codec
- Video & image processing
  - JPEG codec, DCT/IDCT, color space converter
- UARTs
Programmable Solutions Advantages
Spartan-IIIE Enhances Advantages of Programmable Logic

- Time-to-Market
- Flexibility
- Field Upgradable
- Cost Competitive
Xilinx Programmable Solutions Provide Several Benefits

• Accelerating time-to-market
  – Consumer devices require fast time-to-market
  – ASICs & ASSPs take 12-18 months to spin out
    • Immediate production upon design release
  – Fast design iterations
  – Rich, IP portfolio and efficient tools for design and synthesis

• System integration

• Testing and verification
  – Re-programmable means avoiding/reducing risk
  – Solutions are built on a proven FPGA technology with pre-verified silicon and IP that guarantees performance
Xilinx Programmable Solutions Provide Several Benefits

- Increased flexibility
  - Product customization to meet customer needs
  - Accommodate multiple standards & spec updates/changes
  - Feature upgrades through field upgradability (IRL)
    - Remote update of software and hardware
    - Increased lifetime for a product (time-in-market) and allows new, interesting applications
    - Enable product features per end user needs
  - Broad product line
  - Broad IP and tools solutions
Xilinx Programmable Solutions Provide Several Advantages

• Issues in creating a stand-alone ASIC/ASSP
  – Which standards and formats will win in which geographies?
  – Choosing the right solution: over-design or under-design
  – Product customization
  – Development cost and amortization
• System cost management and assured source of supply
  – Multiple sourcing for key high $ BOM components
  – Reduced support costs via IRL
  – Commodity component flexibility
  – Programmable logic solutions are standard parts
• Low cost
PLD Development Flow Advantages
Accelerating Time-to-Market, Extending Time-in-Market

- Time-to-Market advantage
  - First to market increase market share and revenue advantage
- Time-in-Market advantage
  - Maintains/extends competitive position
  - Can greatly increase lifecycle revenue yield
Xilinx Solutions for Digital TVs

- High-speed image/signal processing needs, coupled with large bandwidth requirements of HDTV can be met with low-cost Spartan-IIIE FPGAs with LVDS I/O
- Image processing can be done real-time in FPGAs
  - Cuts down on memory requirements
- Numerous standards (and versions) cause uncertainty so designs need flexibility
  - Transmission schemes, MPEG profiles, display formats, color correction etc.
- Xilinx FPGAs can differentiate your product from the competition while still conforming to the latest revision of standards
- Spartan-IIIE FPGAs offer flexible, cost-effective solutions to ASSPs
- Faster time-to-market and longer time-in-market