Xilinx Solutions for Medical & Scientific
The Xilinx Value Proposition

To enable worldwide customers to attain the fastest time-to-market and flexible product life cycle management by focusing on programmable logic solutions consisting of industry leading silicon, software and IP, and services resulting in a financially sound company.

XILINX®
Xilinx in Industrial, Medical & Scientific

- Industrial market – a key focus for Xilinx
  - Most stable portion of our business
- Broad base of customers worldwide
Medical Equipment and Instrumentation

- Imaging
  - Ultrasound, X-Ray, MRI, CT, nuclear

- Cardiac rhythm mgmt
  - ICDs, external defibrillators

- Home health
  - Breath alcohol testers, cholesterol level monitors, emergency ventilators

- Hospital equipment
  - Patient monitors
  - Dialysis machines
  - Infusion pumps
  - Endoscopy
  - Optometric
  - Powered beds
  - Physiotherapy equipment
  - Powered surgical instruments
Scientific and Lab Instrumentation

- Spectrometers
- Spectrophotometers
- Chromatography
- Sterilizers and autoclaves
- Centrifuges
- Incubators
- Laboratory balances
Issues & Requirements

• Image quality
  – Diagnosis often heavily based on captured images
  – Very high-resolution images need lots of processing power
    • Filtering for noise removal and enhancement

• Real-time digital processing
  – Doctors don’t have to wait for film processing anymore
  – Can perform real-time image adjustments to aid investigations

• Keep it digital!
  – A-D and D-A conversion processes kept to a minimum to keep image quality high
  – Novel image processing techniques easier in digital domain
Experimenting with Tradeoffs

- It would be nice to have a fully flexible device to use for video processing designs
  - Allows changing of parameters like colour depth, bit accuracy (truncation)
  - Allows exploration of new compression techniques or acceleration of existing algorithms to improve throughput
  - Supports various frame rates and resolutions
  - Implements a wide range of new or existing filters for enhancement or noise reduction
Welcome to Xilinx FPGAs

- FPGAs are a key enabling technology for digital video processing
- Allow experimentation for prototypes leading to differentiation for production
- And still enable a higher level of system integration with support for
  - Video interfaces, LAN/WAN technologies, other DSP, simple glue, memory control and state machines, backplane protocols...... the list is only limited by the imagination
Product Solutions

A New Class of CPLDs, The RealDigital CPLD
Low Power, High Performance and Fast Time-To-Market One Cost Effective Solution

Technology and Flexibility You Demand With the Value You Deserve
The Best Combination of Performance and Price

The Ultimate Platform for System Integration and Risk Free Cost Reduction
Redefining the FPGA
Introducing Spartan-3

Xilinx’ Latest Solution for the Medical and Scientific Markets
The Spartan-3 Platform:
A New Class of Spartan FPGAs

- High Performance Sync Dual-Port™ RAM
- 90 nm
- Advanced FPGA Logic with Staggered Pad Technology
- Embedded XtremeDSP Functionality
- SelectIO™-Ultra Technology
- DCM™ Digital Clock Management
- XCITE Digitally Controlled Impedance Control

Alliance CORE LogiCORE™
ISE5 XPERTS
Xilinx Global Services

11
Highest Density with Low Cost
90 nm Process Delivers Higher Yields at Higher Densities

“The companies that get into 90nm production first will get a tremendous advantage in lower cost….. Rivals who are late in 90nm process technology will fall behind and may not be able to catch up.”

Dan Hutcheson
VLSI Research, Inc.

- Faster performance
- Large density devices
- Lower cost devices
# Spartan-3 Product Matrix

<table>
<thead>
<tr>
<th>Device</th>
<th>XC3S50</th>
<th>XC3S200</th>
<th>XC3S400</th>
<th>XC3S1000</th>
<th>XC3S1500</th>
<th>XC3S2000</th>
<th>XC3S4000</th>
<th>XC3S5000</th>
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<tbody>
<tr>
<td>System Gates</td>
<td>50K</td>
<td>200K</td>
<td>400K</td>
<td>1000K</td>
<td>1500K</td>
<td>2000K</td>
<td>4000K</td>
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<td>Logic Cells</td>
<td>1,728</td>
<td>4,320</td>
<td>8,064</td>
<td>17,280</td>
<td>29,952</td>
<td>46,080</td>
<td>62,208</td>
<td>74,880</td>
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<td>Dedicated Multipliers</td>
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<td>12</td>
<td>16</td>
<td>24</td>
<td>32</td>
<td>40</td>
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<td>104</td>
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<td>Block RAM Blocks</td>
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<td>12</td>
<td>16</td>
<td>24</td>
<td>32</td>
<td>40</td>
<td>96</td>
<td>104</td>
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<tr>
<td>Block RAM Bits</td>
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<td>216K</td>
<td>288K</td>
<td>432K</td>
<td>576K</td>
<td>720K</td>
<td>1,728K</td>
<td>1,872K</td>
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<td>Distributed RAM Bits</td>
<td>12K</td>
<td>30K</td>
<td>56K</td>
<td>120K</td>
<td>208K</td>
<td>320K</td>
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<td>DCMs</td>
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<tr>
<td>Max Differential I/O</td>
<td>56</td>
<td>76</td>
<td>116</td>
<td>175</td>
<td>221</td>
<td>270</td>
<td>312</td>
<td>344</td>
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<tr>
<td>Max Single Ended I/O</td>
<td>124</td>
<td>173</td>
<td>264</td>
<td>391</td>
<td>487</td>
<td>565</td>
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<tr>
<td>TQ144</td>
<td>22x22mm</td>
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<tr>
<td>PQ208</td>
<td>30.6x30.6mm</td>
<td>124</td>
<td>141</td>
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<td>FG900</td>
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<td>565</td>
<td>633</td>
<td>633</td>
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</tbody>
</table>
## Spartan-3 Summary

<table>
<thead>
<tr>
<th>Spartan-3 Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Fabric and Routing, Up to 5,000,000 System Gates</td>
<td>Allows for implementation of system level function blocks, high on-chip connectivity and high-throughput</td>
</tr>
<tr>
<td>BlockRAM - 16K Blocks</td>
<td>Enables implementation of large packet buffers/FIFOs, line buffers</td>
</tr>
<tr>
<td>Distributed RAM</td>
<td>For implementing smaller FIFOs/Buffers, DSP coefficients</td>
</tr>
<tr>
<td>Shift Register Mode (SRL16E)</td>
<td>16-bit Shift Register ideal for capturing high speed or burst mode data and to store data in DSP and Encryption applications</td>
</tr>
<tr>
<td>Dedicated 18 x 18 Multiplier Blocks</td>
<td>High speed DSP processing; Use of multipliers in conjunction with fabric allows for ultra-fast, parallel DSP operations</td>
</tr>
<tr>
<td>Single-ended Signaling - GTL, GTL+, PCI; HSTL-I, II, III; SSTL3-I, II; SSTL2-I, II;</td>
<td>Connectivity to commonly used chip-to-chip, memory (SRAM, SDRAM) and chip-to-backplane signaling standards; eliminates the need for multiple level translators</td>
</tr>
<tr>
<td>Differential Signaling (up to 622 Mbps) - LVDS, BLVDS, Ultra LVDS, RSDS, LDT</td>
<td>Differential signaling at low cost - Bandwidth management (saving the number of pins), reduced power consumption, reduced EMI, high noise immunity</td>
</tr>
<tr>
<td>Digital Clock Management (DCM)</td>
<td>Eliminate on-chip &amp; board-level clock delay, simultaneous multiply and divide, reduction of board-level clock speed and no. of board-level clocks, adjustable clock phase for ensuring coherency</td>
</tr>
<tr>
<td>Global routing resources</td>
<td>Distribution of clocks and other signals with very high fanout throughout the device</td>
</tr>
<tr>
<td>Programmable output drive</td>
<td>Improves signal integrity; achieving right tradeoff between TCO and ground bounce</td>
</tr>
</tbody>
</table>
PLD Application Trends

- **Glue Logic**: Counters, Adders, Memory, Controllers, uControllers
- **SSI/MSI**: Data Path, Memory, Controllers, uControllers
- **LSI**: PCI/PCI-X, FEC, FFT/FIR Filters, IMA (ATM), Encryption, MP3 Decoder
- **ASSP App.**: High Volume Apps.
- **Industrial**: Medical Imaging, Test and Measurement, Industrial Automation, Control systems
- **Consumer**: Set-Top Boxes/HDTVs, Telematics, Home Networking
- **Networking**: xDSL Modems, Line Cards
- **Computers**: Graphic Cards, Printers

- **Performance & Density**: 1980s, 1990s, 2000s
- **7400 Series**
FPGA Price Reduction

Price of 100K FPGA Gates Over Time

10,000% Reduction
Enabling High-Speed DSP

Conventional DSP/Software
- Fixed inflexible architecture
  - Typically 1-4 MAC units
  - Fixed data width
- Serial processing limits data throughput
  - Time-shared MAC unit
  - High clock frequency creates difficult system challenge

Example: 256 Tap FIR Filter = 256 MAC operations per sample
256 MAC operations in 256 clock cycles in DSP!!

FPGA Performance Advantage
- Flexible architecture
  - Distributed DSP resources (LUT, registers, multipliers, & memory)
- Parallel processing maximizes data throughput
  - Support any level of parallelism
  - Optimal performance/cost tradeoff

Example: 256 Tap FIR Filter = 256 MAC operations per sample
All 256 MAC operations in 1 clock cycle in FPGA!!
Unrivaled DSP Performance per Dollar

• Nearly 3 billion MACs/sec per dollar
• Cost effective solution for low cost DSP applications such as:
  – Digital communications, video/imaging, & industrial control
• Simple design flow
  – MathWorks (MATLAB/Simulink)
• Complete DSP solution
  – Silicon, software, IP, services, specialists & development systems
The Best of Both Worlds

- Off the shelf devices
- Faster time-to-market
- Rapid adoption of standards
- Real-time prototyping

- Parallel processing
- Support high data rates
- Optimal bit widths
- No real-time software coding

Flexibility of DSP Processors

Performance of Custom ICs

Xilinx DSP Solutions Offer the Best of Both Worlds at a Low Cost!
Basic Image Processing

Scaling

• Fractionally enlarges the incoming data stream as necessary to match the target display resolution
• Pixel processing on-the-fly during image input without frame buffer
Real-Time Image Resizing
With Low Memory Requirements 2 Dimensional Architecture
Upscaling by 2, Downscaling by 4

- Example: 512 x 512 x 8 60 f/s
  - Upscaling by 2, downscaling by 4
  - 16 pixel resolution
  - 8 Block RAMs for line buffers and coefficient bank
  - 4 vertical multipliers
  - 4 horizontal multipliers
  - Adder trees
  - Control

Real-Time Image Rotation

• Non-real time typically implemented using processor and frame store
• Real-time image rotation performed using bi-cubic function in FPGA
  – Pixels remapped to rotational co-ordinates
Real-Time Image Rotation

• Medical imaging example
  • 1024 x 1024 x 12 @ 30 f/s
  • 40 MHz Pixel Clock
  • 160 MHz Core Clock

  - Xilinx XC2S300E FPGA
    • 12 Block RAMs for line buffers
    • 2 Block RAMs for RC lookup tables
    • 5 multiplier pixel calculation
    • Sine/cosine, 2 Block RAMs
    • Dx, Dy calculation
    • Sx, Sy calculation
    • Control

$S_x = Dx \cos(\theta) + Dy \sin(\theta)$
$S_y = -Dx \sin(\theta) + Dy \cos(\theta)$

Xilinx Color Space Converter

- Free of charge Reference Design available “as is”
- For more details check out http://www.xilinx.com/xapp/xapp283.pdf
R’G’B’ to Y’CbCr Converter

- Free of charge Reference Design available “as is”
- For more details check out http://www.xilinx.com/xapp/xapp637.pdf
# MPEG IP for Xilinx FPGAs

<table>
<thead>
<tr>
<th>IP Core or Reference Design</th>
<th>Provider</th>
</tr>
</thead>
<tbody>
<tr>
<td>XAPP610 Video Compression using DCT</td>
<td>Xilinx Inc.</td>
</tr>
<tr>
<td>XAPP611 Video Compression using IDCT</td>
<td>Xilinx Inc.</td>
</tr>
<tr>
<td>XAPP208 IDCT Implementation in Virtex</td>
<td>Xilinx Inc.</td>
</tr>
<tr>
<td>2-D DCT</td>
<td>Xilinx Inc.</td>
</tr>
<tr>
<td>1-D DCT</td>
<td>Xilinx Inc.</td>
</tr>
<tr>
<td>2-D DCT</td>
<td>eInfochips</td>
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<tr>
<td>2-D DCT/IDCT</td>
<td>BARCO-SILEX</td>
</tr>
<tr>
<td>2-D IDCT</td>
<td>CAST Inc.</td>
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<td>2-D DCT</td>
<td>CAST Inc.</td>
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<tr>
<td>2-D DCT/IDCT</td>
<td>CAST Inc.</td>
</tr>
<tr>
<td>DCT/IDCT</td>
<td>TILAB</td>
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<tr>
<td>MPEG-2 SDTV I &amp; P Encoder</td>
<td>Duma Video</td>
</tr>
<tr>
<td>MPEG-2 HDTV I &amp; P Encoder</td>
<td>Duma Video</td>
</tr>
</tbody>
</table>

See [www.xilinx.com/ipcenter](http://www.xilinx.com/ipcenter) for more details
Chroma Downsampling

- Most MPEG-2 applications use 8-bit 4:2:0 sampling
- But incoming data usually 10-bit 4:2:2 video
  - Maybe via SDI (Serial Digital Interface) for example
- Conversion therefore needed before processing
  - Easy implementation using high-speed FIR filters in FPGA
Picture Enhancement

Easily implemented in FPGA
Spatial Enhancement

• Endless list of enhancement algorithms:
  – Spatial Filter Unsharp Masking
  – Digital Max-Detail
  – Laplacian of Gaussian Filter
  – Adaptive Histogram Equalization
  – Adaptive Kalman Temporal Filter
  – Non-Linear Median Filter
  – Non-Linear Fuzzy Filter

• Or you may have a better version of your own
  – Is there an ASSP to support your idea?

• Reprogrammable FPGAs allow for experimentation in research and development
  – Leads directly to differentiation in production
FPGAs for Spatial Enhancement

+ User selectable kernels
+ Experiment to find the filter that gives the best results (on-the-fly)
+ Parameterizable filter coefficients and windows
+ No sacrifice in performance with real-time calculations possible
Spatial Enhancement

\[(H \times \text{Original}) - (K \times \text{Low_pass_filter}) = \text{Enhanced Image}\]
FIR Filters for Xilinx FPGAS

- Most image filtering can be done based on two-dimensional FIR filters
  - Programmability allows experimentation with different coefficients, filter windows, etc to get the best results

<table>
<thead>
<tr>
<th>IP Core or Reference Design</th>
<th>Provider</th>
</tr>
</thead>
<tbody>
<tr>
<td>XAPP219 Transposed Form FIR Filters</td>
<td>Xilinx Inc.</td>
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<tr>
<td>MAC FIR</td>
<td>Xilinx Inc.</td>
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<td>Serial Distributed Arithmetic FIR Filter</td>
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<td>Parallel Distributed Arithmetic FIR Filter</td>
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<tr>
<td>Distributed Arithmetic FIR Filter</td>
<td>Xilinx Inc.</td>
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</tbody>
</table>

See http://www.xilinx.com/ipcenter for more details
FPGA Features for Video

- Analog Video Decoder
- RGB Video
- A/D Converter
- Optional Digital Decode
- Analog Video
- RGB Video
- PHY
- - 1394
- - USB 2.0
- - Ethernet
- - TMDS
- - LVDS
- - PCI
- - Etc.

FPGA Display System Utility

- SDRAM
- SRAM
- FLASH
- Hard Disk
- Select I/O
- Display Driver
- Select I/O
- uC
- MicroBlaze
- Image Processing
- Decode & Decrypt
- DCT
- IDCT
- JPEG
- DES
- AES
- 3DES
- PCI
- PCI-X
- AGP
- LVDS / BLVDS
- Select I/O
- PCI
- PCIX
- AGP
- Etc.

- 2D FFT
- YCoCg2RGB
- RGBYUV
- YUV2RGB
- 2D FIR Filter
- RGB2YCrCb
- YCrCb2RGB
- YUV2RGB
- DES
- AES
- 3DES
- PCI
- PCI-X
- AGP
- Etc.
X-Ray System Example
Ultrasound Beamformer

Legend:
- Xilinx
- Memory
- CPU
- Non-Xilinx
- Mixed Signal
- Embedded Logic

Audio Output

Medical Display

Beamformer Central Control
RX Beamformer
- Color Doppler Processing
- Image & Motion Processing
- Spectral Doppler Processing

HV TX Amps
MUX & Transducer Switch
TX Beamformer
TGC Amplifier
ADC
Data Acquisition Card

- Analog IN Ch. 1:
  - 14-bit A/D
  - 6 pole Elliptic Filter
- Analog IN Ch. 2:
  - 16-bit D/A
  - 6 pole Elliptic Filter
- Trigger:
  - A/D Start Trigger
  - A/D Stop Trigger
  - D/A Start Trigger
  - D/A Stop Trigger

Legend:

- Xilinx
- Memory
- CPU
- Non-Xilinx
- Mixed Signal
- Embedded Logic
Smart Vision System

Legend
- Xilinx
- Memory
- CPU
- Non-Xilinx
- Mixed Signal
- Embedded Logic

External I/F (PCI, LVDS, etc.)
Feedback Control
Pixel Processing
Feature Extraction
Image Acquisition
CCD Sensor
High Speed Pattern Recognition

Feedback
Host System
SRAM
Digital Communications

- Remote diagnosis possible
  - Even remotely controlled procedures
  - Needs huge bandwidth for real-time analysis
- Off-site/central archiving of digital patient files
  - Requires integration of datacom/telecom interfaces
  - Storage Area Network protocols may play a role
- Xilinx supports a wide range of interfaces and protocols to enable focus on the real system value add

For more on protocols and backplanes: www.xilinx.com/esp/optical/net_tech
Xilinx - the Ultimate Connectivity Platform

**LAN / MAN / WAN**
- 10/100 Ethernet
- 1Gb Ethernet
- 10Gb Ethernet
- 1Gb Ethernet PHY
- 10Gb Ethernet XAUI
- OC48* OC192* OC768*

**Board-to-Board**
- PCI 32/33
- PCI 64/66
- PCI-X 133
- 3GIO
- Fibre chan.
- 10GE XAUI
- RapidIO
- CSIX
- HyperTransport™
- RapidIO™ Serial
- HyperTransport™

**Chip-to-Chip**
- PCI 32/33
- PCI 64/66
- PCI-X 66 & 133
- RapidIO™
- 10GE XAUI
- POS-PHY L3/L4
- Flexbus 4
- CSIX
- HyperTransport™
- 3GIO

* SONET compatible, supports data rate

Serial Standards – Virtex-II Pro
Parallel Standards – Spartan-3, Spartan-IIE, Virtex-II & Virtex-II Pro
Supporting Legacy & Evolving System Interfaces

- QDR SRAM
- NoBL/ZBT SRAM
- SDR/DDR SDRAM
- FCRAM
- Sigma RAM
- RLDRAm
- CAMs

- PCI 32/33
- PCI 64/66
- PCI-X
- 10/100 Ethernet (MII)
- Proprietary

- 10 Gbit Ethernet - XAUI, XGMII, XAUI
- Proprietary

- RapidIO
- RapidIO Serial
- Infiniband
- 3GIO
- Fibre Channel
- POS-PHY L3/L4
- FlexBus 3/4
- CSIX
- HyperTransport
- SPI4 Phase1, Phase2
- Gigabit Ethernet - GMII
Virtex-II Pro Helps You Manage the Transition from Parallel to Serial I/Fs

Select/O-Ultra™ technology for parallel interfaces
- 25 I/O standards
- XCITE technology
- 840 Mbps LVDS
- Dedicated DDR registers

Rocket I/O Multi-Gigabit Serial Transceivers
Up to Sixteen 3.125 Gbps transceivers

- Helps preserve investment in legacy designs
- Eases transition from parallel to serial technology
- Parallel interface designs will not go away
Lowest Cost Parallel Interconnect Solutions

• Best value in popular cores
  – PCI 32/33 effective cost below 75 cents* ($ .75)
• Physical interfaces and system elements
  – 25 I/O standards, DDR I/O registers, DCMs
• Popular IP cores
  – Pre-engineered, Drop-in functionality
  – Fully compliant, Pre-verified

* Based on pricing for 2004, 250K units
SDI - Serial Digital Interface

- Standard for transporting *uncompressed* standard-definition digital video serially over coax cable
  - ANSI/SMPTE 259M
  - ITU-R BT.656
  - Many related SMPTE and ITU standards and recommended practices
- Xilinx has a set of application notes showing how to implement the SDI protocol
- FPGA-based solutions are *very* competitive with ASSP SDI solutions
SDI Application Notes

XAPP247: SDI Physical Layer Implementation
XAPP248: Digital Video Test Pattern Generators
XAPP288: SDI Video Decoder
XAPP298: SDI Video Encoder
XAPP299: SDI Ancillary Data & EDH Processors
XAPP625: SDI Video Standard Detector & Flywheel Decoder


Coming Soon!

Digital Video

SDI Video Standard Detect & Flywheel

SDI ANC & EDH Processor

SDI Video Encoder

SDI Driver

Video

SDI bitstream

Digital Video Test Pattern Generator

SDI Receiver

SDI Video Decoder

Video Standard Detect & Flywheel

Ancillary Data

Digital Video

Clock
ASSP SDI Implementation

SDI Transmitter

- Digital Video
- Digital Audio
- Audio CODEC
- EDH Processor
- Encoder & Serializer
- SDI Bitstream

$39 $19 $36 $94 total

SDI Receiver

- SDI Bitstream
- Equalization & CDR
- Clk
- Data
- Deserializer & EDH
- Audio CODEC
- Digital Video
- Digital Audio

$36 $28 $39 $103 total
### Xilinx SDI Implementation

#### SDI Transmitter
- **Audio CODEC, EDH Processor, Encoder, Serializer**
- **Cable Driver**
- **SDI Bits stream**
- **Xilinx FPGA**
- **$2**

**SDI Receiver**
- **Equalizer**
- **CDR**
- **Deserializer, Decoder, Framer, EDH Processor, Audio Codec**
- **SDI Bits stream**
- **Xilinx FPGA**
- **$10**
- **$17**

*For fixed operation at 270 Mb/s, CDR can be replaced with $3 ASSP and a DLL in the FPGA (XAPP250)*

**SDI functionality integrated into existing system FPGA gives even more saving**
HD-SDI - High Definition SDI

- Transports *uncompressed* high-definition video serially over video coax cable or fibre
  - 100+ meters of coax cable
  - 2km of single mode fibre
- Two bit rates
  - 1.485 Mb/s
  - 1.485/1.001 Mb/s - primarily used in North America
- Builds upon SDI experience base
  - Encoding, decoding, framing, and equalization are similar
High Def. Video Broadcast Chain

- Satellite Rx
- DVB-ASI HD-SDI
- HD-SDI
- HD-SDTI
- SDI Router
- HD to SD Converter
- SD to HD Converter
- Camera
- VTR
- MPEG-2 Encoder
- MPEG-2 Editing Station
- HD-SDI
- HD-SDI
- HD-SDTI
- DVB-ASI
- DVB-ASI HD-SDI
- DVB-ASI HD-SDTI
- DVB-ASI HD-SDI
- DVB-ASI HD-SDTI
- MPEG-2 Storage
- Video Server
- HDTV Transmitter
- On-Air Production
- SMPTE 310
- HD-SDI
- HD-SDTI
- DVB-ASI
- Firewire DVI
- Set Top Box
- HDTV Monitor
- DVI
- DVI
Virtex-II Pro HD-SDI Tx

Design Concept

- Parallel Video Clock 74.25MHz (/1.001)
- External PLL may be needed to reduce jitter
- Y Channel Data
- C Channel Data
- PLL
- BUFG
- DCM
- CRC
- SMPTE 292 Encoder
- Logic Level Translation
- Rocket I/O Transceiver (8B10B bypassed)
- REFCLK
- TXUSRCLK
- TXUSRCLK2
- TXDATA
- Cable Driver
- 75 ohm Coax
Virtex-II Pro HD-SDI Rx
Design Concept
SDV Demo Board

SD-SDI IN

Cable Equalizer

HD/SD SDI IN

Cable Equalizer

REFCLK Oscillator

DVB-ASI IN

CDR

VCO

SD-SDI IN

CDR

SD-SDI Decoder

SD-SDI Encoder

8B10B Decoder

8B10B Encoder

HD/SD SDI IN

Rocket IO

HD-SDI Decoder

HD-SDI Encoder

Rocket IO

DVB-ASI OUT

Cable Driver

SD-SDI OUT

Cable Driver

HD/SD SDI OUT

Cable Driver

DVB-ASI OUT

Cable Driver
Internet Reconfigurable Logic (IRL)

Remote update of software and hardware

Get your Customers to Market Early

Fix a bug

Enhance Performance

Ensure Compatibility

Internet Reconfigurable Logic (IRL)

Remote update of software and hardware
Value of Remote Upgrades

• Adds key differentiation between competitive products
  – Future-proofs your products
    • Enables instant compliance to new standards
    • Continuous improvement
    • Results in increased lifetime for the gateway
  – Enable product features per end-user needs
  – Large ‘bottom line’ impact
    • Reduce maintenance costs
    • New Internet-based revenue opportunities
  – Increased market share
    • Get in earlier and stay in longer
    • Develop customer loyalty

• ASSPs/ASICs cannot provide this capability
Xilinx FPGAs – The Competitive Edge

- Leverage existing designs/chipset to support multiple geographies
- Faster time-to-market
- Improved inventory control
- Reduce exposure to supply issues
  - Flexibility to efficiently manage component supply problems
- React quickly to competitive pressures
  - Field upgradability
  - Bringing new features/capabilities rapidly to market
Xilinx in Scientific and Medical

• Enables the designer to add real value to the system
  – Experimentation in development leading to differentiation in production
  – Chipsets that support your exact requirements are never available!!

• Supports high-definition real-time processing
  – “Dedicated” logic allows for hardware acceleration of key algorithms
  – Less memory requirements for off-line processing

• System-on-chip integration saves board space and reduces BOM
  – More processing power with less devices
    • Reduction of DSP “farms” using parallel processing capability of FPGA
  – Integration of network and backplane interfaces, display controllers, level translators, clock management, etc.

More white papers on Xilinx FPGAs for image filtering, enhancement and scaling/rotation at
http://www.xilinx.com/xlnx/xil_prodcat_product.jsp?title=literature_training#conference
Questions?

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