Xilinx in the Wired Communications Market
Backgrounder

Enabling Migration to 40G and 100G Network Infrastructure

As the telecommunications market undergoes its current cycle of consolidation following the last decade's explosive growth in capacity, the demands of the Internet continue to push the need for innovation. Today's rapid rise of residential video and advanced business services traffic is causing a spike in bandwidth throughout the global telecommunications network, starting at the access edge of the network and driving up through the Metro network to the core. In response, operators are pushing to higher port rates, which have included 40Gbps SONET (OC-768 and OTU3) and Ethernet (40GE) rates. Increasingly, many operators are pushing rates to 100GE while the IEEE's High-Speed Serial IO working group reaches the final stages of standardizing the 40GE and 100GE specification (IEEE 802.3ba).

Such business and economic dynamics create the mandate for scalable, flexible and cost-effective technical solutions that can meet the evolving requirements and standards of the telecommunications industry. To keep pace with these dynamics, wired communications equipment manufacturers are shifting away from their use of custom-made (ASIC) and off-the-shelf (ASSP) chips, and relying more upon programmable silicon platforms and IP solutions in order to accelerate the deployment of ultra high-bandwidth systems.

The Push to 40GE and 100GE

The impact of the industry's newest ultra high-bandwidth standards will be felt throughout the network, which must now support lucrative legacy services while operators migrate the core to a single, unified infrastructure to keep down operational costs. Encryption and authentication services are now mandatory to secure networks from hackers and catastrophic failures. Advanced traffic engineering capabilities are needed, so manufacturers can more efficiently differentiate and charge for higher-quality classes of end-to-end services.

By the year 2016, the industry's efforts to create 40 and 100GE systems is expected to generate $4.2 billion in annual combined revenues, with initial demand for new solutions coming from large data and switching centers, while new trends such as file and storage virtualization or high-resolution imagery and video will require higher-speed interfaces.[1]

These requirements present extraordinary challenges to system and hardware designers on multiple fronts. They must develop hardware that is capable of migrating from 10G to 40G to 100G with the signal integrity required for reliable operation of 10G/100G links. They must support multiple connectivity protocols, while also adapting to changes in the evolving standard for the interface between 100G optical modules and the media access controller (MAC). And, of course, they must deliver new products to market quickly in order to achieve maximum market share, revenue and profit.

---

[1] Lightwave, April 2008, http://lw.pennnet.com/display_article/325344/13/ARTCL/none/none/1/40/100

Economic Benefits of Programmable Technology

Over the last several years, the role of field programmable gate arrays (FPGAs) in networking and telecom systems development has expanded beyond bridging logic between various components on an integrated circuit board. As they push to advanced technology nodes from 65-nanometer (nm) today to 40nm and beyond, FPGA-based solutions deliver the features, performance and flexibility of a custom chip solution, while offering significantly lower development costs. Compared to ASSPs, FPGAs are most often the only solution available to developers who can't wait for an off-the-shelf solution and still be competitive.

As they fall in cost and improve in density and performance, today's FPGAs are running entire systems and subsystems in end products ranging from the lowest end DSLAMs and Ethernet switches to the highest end core routers and WDM equipment. Not only are designers using programmable devices to prototype these systems, but are increasingly more often taking them into production based largely on FPGAs. This is why the wired communications business continues to be the largest market for Xilinx FPGAs, comprising about 35 percent of the company's revenue over the last few years for a total of about $600 million per year.

Xilinx estimates the market for its wired communications solutions to be over $7 billion for 2008 and growing over 7 percent per year. The company heavily invests in reference designs, intellectual property (IP) and software tools to offer developers of wired communications systems what they need to integrate high-performance Virtex® and low-cost Spartan® series FPGAs into their systems. Xilinx Wired Communications solutions support a wide range of applications, including:

- Transport Market Segment
  - Core: Core Switches, Core Routers, Long Haul Transport DWDM
  - Metro: Metro Switches, Metro Routers, Metro DWDM
  - Edge: Access/Aggregation Switches, Edge Routers, PON (Passive Optical Networks), DSLAMs, Wireless Backhaul

- Enterprise Market Segment
  - Switching
  - Security

Low Risk FPGA Solutions for 40G and 100G Networking

Because of the Virtex-5 family's modular ASMBL™ architecture, Xilinx is able to rapidly and cost effectively deploy FPGA variants to meet specific market requirements as they arise. To help developers quickly prototype and bring to production new products that address the growing market for 100G networks, Xilinx has introduced the Virtex-5 TXT FPGA platform with supporting IP and development tools.

The Virtex-5 TXT FPGA platform consists of two devices that deliver a mix of logic cells and block RAM with the highest density of high-speed transceivers available for any FPGA. With up to 48 RocketIO™ multi-rate transceivers running at 6.5Gbps (twice as many as Virtex-5 FXT FPGAs), Virtex-5 TXT devices deliver the 600Gbps total

bandwidth required for building network bridges. Because these devices are based on the same silicon blocks that are the foundation of other Virtex-5 FPGA platforms, the embedded transceivers have been fully characterized by Xilinx and field-proven by customers.

Virtex-5 TXT FPGA Platform			
Part Number		XC5VTX150T	XC5VTX240T
Slices (2)		23,200	37,440
Logic Cells (3)		148,480	239,616
CLB Flip-Flops		92,800	149,760
Maximum Distributed RAM (Kbits)		1,500	2,400
Block RAM/FIFO w/ECC (36kbits each)		228	324
Total Block RAM (kbits)		8,208	11,664
Digital Clock Manager (DCM)		12	12
Phase Locked Loop		6	6
Maximum Single-Ended Pins (4)		680	680
DSP48E Slices		80	96
PCI Express Endpoint Blocks		1	1
10/100/1000 Ethernet MAC Blocks		4	4
RocketIO™ GTX High-Speed Transceivers		40	48
Package (7,8)	Area		
FFA Packages (FF): flip-chip fine-pitch BGA (1.0 mm ball spacing)			
FF1156	35 x 35 mm	360 (40)	
FF1759	42.5 x 42.5 mm	680 (40)	680 (48)

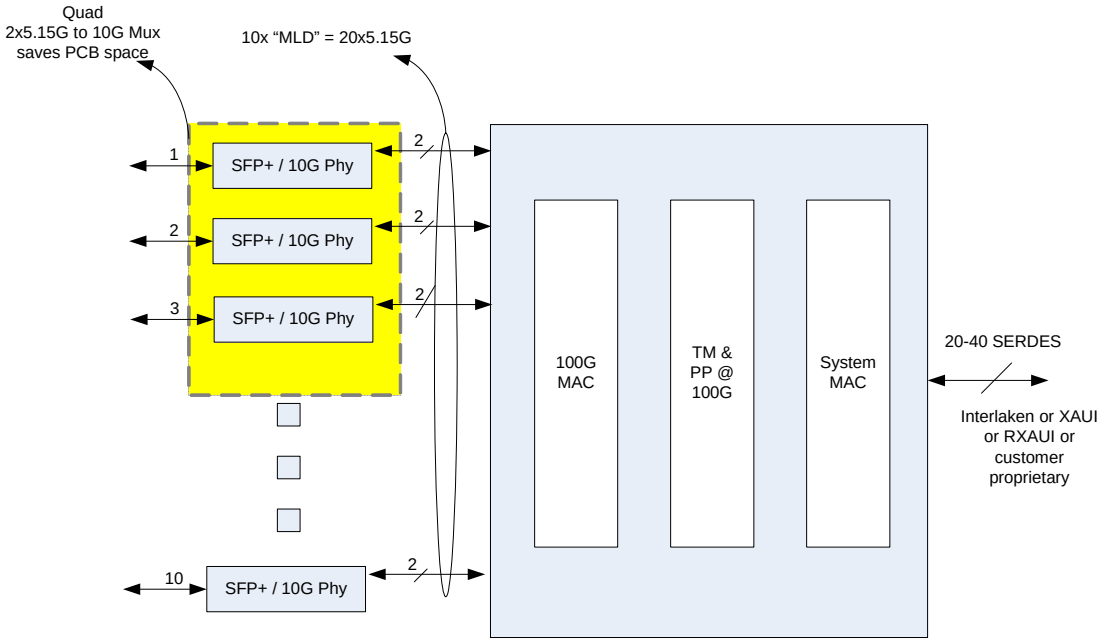
100Gigabit Ethernet MAC to System Interface Bridge

Xilinx works closely with standards organizations as well as other IP and silicon vendors throughout the telecommunications industry ecosystem to deliver solutions that support XAUI, RXAUI, Interlaken, SONET, ODN and many other wired standards.

Xilinx collaborated with Sarance Technologies to provide the industry's first 100GE MAC solution, a full featured, IEEE 802.3ba compliant solution implemented with Virtex-5 FPGAs. It is up and running today on Tier 1 vendor hardware prototypes using two Virtex-5 FXT FPGAs, 10 external 10Gbps PHYs, and a variety of system side interfaces.

The 100GE MAC-to-Interlaken bridge solution supported by the new Virtex-5 TXT FPGA platform offers a very low risk option for condensing functionality into a single FPGA and three external Quad SERDES Muxes. This implementation includes Xilinx

exclusive 64/66 and 64/67 encode/decode gearboxes built into the GTX transceiver that save nearly one-fifth of the logic count and power consumption of the design.



At the Leading Edge of Innovation

The new Virtex-5 TXT FPGA platform is built upon the experiences of developers who have used Virtex-5 devices to support new ultra high-bandwidth systems. In November of 2006, Xilinx FPGAs were used to showcase the world's first successful 100GE transmission through a live production network demonstrated at SC06 International Conference, the premier international conference of high performance computing, networking, storage and analysis. Finisar teamed with Level3 Communications, Internet2, and the University of California at Santa Cruz (UCSC) to demonstrate the transmission of 100GE traffic over the Level3 DWDM network from the show site in Tampa, FL, to Houston, TX, and back — a total of 4,000 miles. The Xilinx FPGA electrically transmitted all ten signals to ten 10Gbps XFP optical transceivers, which converted the signals into the optical domain. From there, the signals were transmitted to Infinera's commercially available DTN Switched WDM System, where they were handed off to the Level3 network.[2]

In June of 2008, telecommunications giant Comcast Corporation announced the successful completion of a 100GE technology test over its existing backbone infrastructure between Philadelphia and McLean, VA using the industry's first 100GE router interface. The system used the same Sarance Technologies' High Speed Ethernet IP Core (HSEC) running on a Virtex-5 FXT FPGA that is supported by the Virtex-5 TXT platform today.

[2] Lightwave, January 2007, http://lw.pennnet.com/display_article/281527/13/ARTCL/none/none/1/Indust

Summary

Programmable system solutions offer a low-cost, low-risk path to developing a wide variety of applications in the wired telecom market. The performance of the FPGA fabric has evolved to support even the highest-performance 100Gbps applications. As the market leader in FPGAs, Xilinx listens closely to customer and market requirements, and engineers its silicon, software and FPGA IP to offer the right solution at the right time – enabling the economies of scale, flexibility and increase in quality of service delivery needed for the wired telecom industry's migration to 100GE.

For more information about Xilinx Solutions for the Wired Telecom Market, please visit: http://www.xilinx.com/esp/wired.htm