

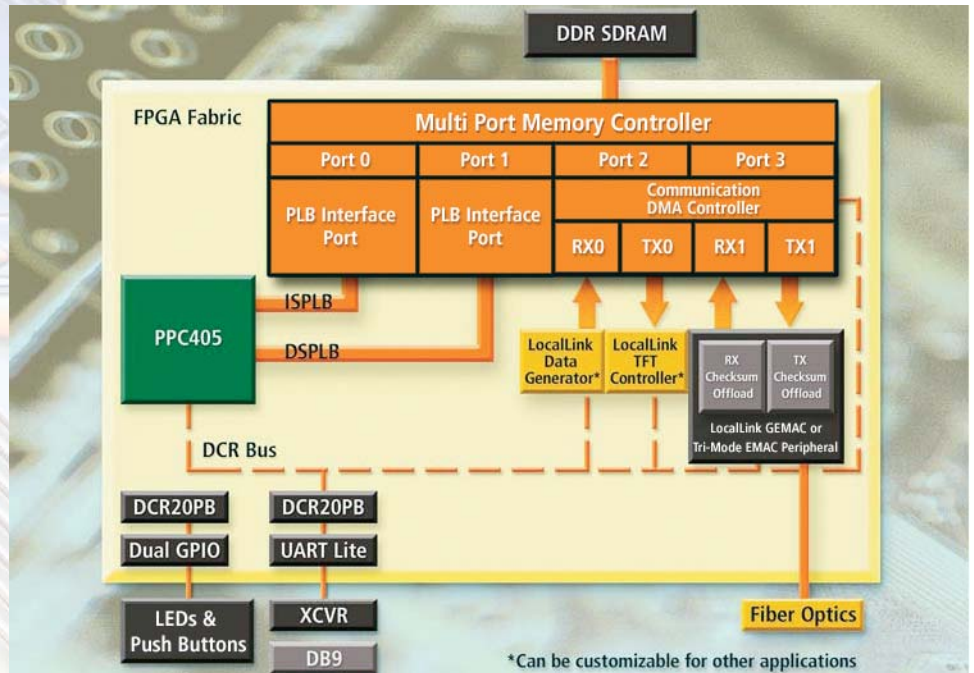


Xilinx Gigabit System Reference Design (GSRD)

With Hardware Checksum Offload and Zero-Copy

Networked systems requiring large amounts of memory bandwidth often face significant challenges in managing overall system performance. The Xilinx Gigabit System Reference Design (GSRD) is a high-performance Gigabit Ethernet system design built on the Xilinx Virtex™-4 FX and Virtex-II Pro FPGAs. The design enables you to use the Virtex-4 FX or Virtex-II Pro in conjunction with its embedded PowerPC to terminate IP-based transport protocols such as TCP or UDP.

The GSRD removes the need for costly software copy and checksum operations by the host CPU, leaving the PowerPC to process only the headers of TCP/IP and related protocol packets. This design provides high-performance bridging between IP-based protocols and user-data interfaces. The system incorporates a Multi Port Memory Controller (MPMC) and a Communication Direct Memory Access Controller (CDMAC) as the infrastructure to move large data between the Ethernet controller and memory while providing sufficient memory bandwidth to the CPU and other peripherals.



• Programmable for TCP and UDP Processing

The GSRD removes the processor from the payload data path, an important consideration for embedded Gigabit systems. The processor executes only the protocol and control functions, leaving data transfer to the DMA engines. The data realignment and the checksum-offload features provide the support necessary for zero-copy functionality to be implemented in software. This makes the design suitable for high-performance bridging between IP-based protocols and user-data interfaces.

• Increased System Bandwidth

The design leverages the MPMC and CDMAC to improve memory bandwidth between the instruction and data PLB interfaces of the PowerPC and data ports. Each data port has two built-in DMA engines with data realignment. One data port of the GSRD connects to a Gigabit Ethernet MAC (GEMAC) or Tri-Mode Ethernet MAC (TEMAC) while the other data port can be used to connect additional peripherals to the system. Both the data ports and the DMA engines are controlled via the Device Control Register (DCR) bus of the PowerPC.

• Typical Applications for the GSRD

- TCP/IP Termination
- Storage Solutions: iSCSI Bridging
- IP over Gigabit Ethernet Switch
- High-Speed Remote Monitoring/Control over IP Networks
- Reliable Remote Image/Video Capture

System-Level Features

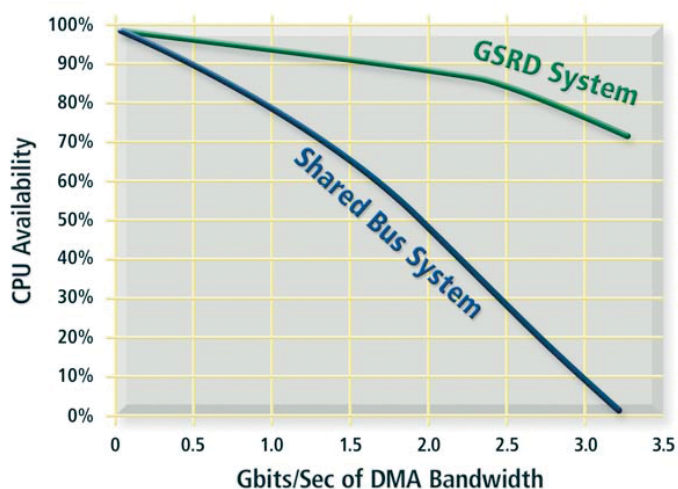
- Available for ML300, ML310 and ML403 Evaluation Platforms
- Multi Port Memory Controller (MPMC) for DDR SDRAM
- Communication DMA Controller (CDMAC)
- LocalLink Gigabit Ethernet MAC Peripheral (LL_GEMAC)
- LocalLink Tri-Mode Ethernet MAC Peripheral (LL_TEMAC)
- Verilog source code
- Linux Port Available
- Netperf under Linux
- Evaluation Treck TCP/IP stack linkable library

Multi Port Memory Controller (MPMC)

The MPMC allows the 32-bit DDR SDRAM memory resource to be shared over four independent interface ports. Each of these ports permits full read and write access from the CDMAC and PowerPC. Each MPMC port is implemented as a point-to-point connection rather than a shared bus, thus permitting higher performance.

- 32-bit DDR200 Memory Interface
- Four Ports
- Per-Port Personality Modules (PLB, CDMAC)
- Per-Port Bidirectional Rate Matching FIFOs
- Intelligent Arbitration for Memory Resource

Shared Bus vs. GSRD CPU Availability



Communication DMA Controller (CDMAC)

The CDMAC manages the flow of data between communication devices and memory. It supports variable packet sizes and can transfer data to/from memory addresses with byte resolution. CDMAC control and status registers are available via the DCR interface of the PowerPC 405. This frees up the high-speed ports to be used solely for data transfer.

- Four DMA Engines
- LocalLink Interface
- 128 Byte Memory Burst Size
- Unrestricted Data Buffer Alignment
- User Data Fields in Buffer Descriptors Accessible Through LocalLink

LocalLink Gigabit Ethernet MAC and LocalLink Tri-Mode Ethernet MAC Peripherals

The LocalLink Gigabit Ethernet MAC (LL_GEMAC) and LocalLink Tri-Mode Ethernet MAC (LL_TEMAC) peripherals provide a Gigabit Ethernet interface. These peripherals use a streaming interface – the Xilinx LocalLink interface. LocalLink is a packet streaming interface for communication devices that provides a simple protocol to transfer data in a single direction. The LL_TEMAC can use either the Virtex-4 FX Embedded Tri-Mode Ethernet MAC or the Tri-Mode MAC LogiCORE. The LL_GEMAC uses the 1-Gigabit Ethernet MAC LogiCORE. All the Ethernet MACs that are used by the LocalLink peripherals have been UNH tested.

- TCP and UDP Checksum Offload on Transmit and Receive data paths
- Zero-Copy
- Supports Jumbo Frames
- LocalLink Interface to CDMAC
- Based on UNH tested Xilinx Gigabit Ethernet MAC LogiCORE and Xilinx Tri-Mode Ethernet MAC LogiCORE
- RocketIO™ Interface Directly Drives Gigabit Ethernet Optical Transceivers

Take the Next Step

For more details on the Xilinx Gigabit System Reference Design (GSRD), visit www.xilinx.com/gsr

The GSRD application note (XAPP536) is available at www.xilinx.com/bvdocs/appnotes/xapp536.pdf

The MPMC application note (XAPP535) is available at www.xilinx.com/bvdocs/appnotes/xapp535.pdf

Using the Treck Embedded TCP/IP Stack application note (XAPP546) is available at www.xilinx.com/bvdocs/appnotes/xapp546.pdf

Corporate Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Tel: (408) 559-7778
Fax: (408) 559-7114
Web: www.xilinx.com

European Headquarters

Xilinx
Citywest Business Campus
Saggart,
Co. Dublin
Ireland
Tel: +353-1-464-0311
Fax: +353-1-464-0324
Web: www.xilinx.com

Japan

Xilinx, K.K.
Shinjuku Square Tower 18F
6-22-1 Nishi-Shinjuku
Shinjuku-ku, Tokyo
163-1118, Japan
Tel: 81-3-5321-7711
Fax: 81-3-5321-7765
Web: www.xilinx.co.jp

Asia Pacific

Xilinx Asia Pacific Pte. Ltd.
No. 3 Changi Business Park Vista, #04-01
Singapore 486051
Tel: (65) 6544-8999
Fax: (65) 6789-8886
RCB no: 20-0312557-M
Web: www.xilinx.com

Distributed By:

FORTUNE 2005
100 BEST COMPANIES TO WORK FOR


The Programmable Logic Company™