IEEE802.16 WirelessMAN Solutions
Xilinx is #1 FPGA supplier to Wireless Infrastructure

• Xilinx is the #1 programmable logic supplier to the Wireless Infrastructure industry
• Xilinx FPGAs used by all the Major Base Station Vendors
• First Wireless Design Win in 1986
  – Dramatic ramp up from 1995 to present
Current Fixed Wireless Access Markets

• Wide range of Fixed Wireless Access systems available today
  – all designed to meet different market needs

• Many proprietary schemes used by different vendors in each of the markets
  – Seen as a hindrance to market growth
  – Growth rates have not met projections

• Convergence and standardization now seen as the future
Multipoint Microwave Distribution Systems (MMDS)

- Originally used for analog TV transmission
  - 33 analog video channels, each 6 MHz wide
- New implementations
  - 99 digital, data streams, each transmitting at 10 Mbps
- Only 200MHz spectrum between 2.5 and 2.7GHz
- Either Line-of-Sight or Non-Line-of-Sight with a greater range than LMDS

Worldwide MMDS Subscriber and Service Provider Revenue Forecasts (x 1,000)

Source: Cahners In-Stat Group
Local Multipoint Distribution Services (LMDS)

- Provides high speed video, data and internet access
  - The primary means of delivering fixed wireless service to end-users in the United States
  - Bulk of deployment targeted at extending fiber infrastructure to major markets
- Line-Of-Sight with no greater than a three-to-five mile range
  - Operates in 28GHz & 29GHz bands

Worldwide LMDS and Subscriber and Service Provider Revenue Forecast (x 1,000)

Source: Cahners In-Stat Group
A changing market

• Supply of services to consumer not generally seen as viable against competition from cable and ADSL
  Except:
  – Services to consumers in shared residential complexes such as tower blocks
  – Emerging economies with little or poor existing wired services in Asia, Africa and South America

• Now concentrating on cellular back-haul networks and small/medium business services
Broadband Fixed Wireless Network Diagram

Figure courtesy of Alcatel
Differences between Fixed and Mobile Wireless Networks

- Unlike Mobile Networks, Fixed Wireless Networks do not have to deal with transmission problems caused by the terminal moving
  - No Doppler problems
  - No Handover to adjacent cell problems
  - Simpler power management and control
- At the system level Fixed Wireless systems are less complex than Mobile systems, however:
  - the high data rates in Fixed Wireless makes the system design as challenging at the baseband level
Broadband Wireless Internet Forum (BWIF) Proposal

- Proposes interoperable systems based on Vector Orthogonal Frequency Division Multiplexing (VOFDM) modulation and cable-modem DOCSIS protocols
- 51 member companies
  - Including Cisco, Spike Broadband, Pace, Vyyo, Piping Hot
- Optimized for Non-LOS conditions and currently operates in 5.7 GHz and 2.5GHz bands
- Designed primarily to compete with Cable and ADSL access
- More details at: http://www.bwif.org
ETSI HiperAccess™ & HiperMAN™

- Share many features of HiperLAN
- HiperAccess
  - >11GHz carriers
  - Line of Sight connections, up to 5 miles range
  - 25 - 60 Mbit/s data rates, using Single Carrier
- HiperMAN
  - <11GHz carriers
  - Doesn’t need Line Of Sight, up to 15 miles range
  - 10- 25 Mbit/s data rates, using OFDM
- Harmonization efforts under way to have degree of compatibility with 802.16
IEEE 802.16 WirelessMAN™

- USA specification designed to provide the "first-mile/last-mile" connection in wireless metropolitan area networks
- Bandwidth between 10 and 66 GHz
  - 2 to 11 GHz region due to be added during 2002
- Supports continuously varying traffic levels
  - 54 Mbps data per channel
- Uses different modulation schemes depending on type of data and error rates etc.
## Comparison of IEEE802.16 and HiperAccess

<table>
<thead>
<tr>
<th>Standards</th>
<th>ETSI-BRAN</th>
<th>IEEE 802.16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Access</td>
<td>FDD primary choice, TDD for unpaired bands. TDMA (u/d) / TDM (d)</td>
<td>Mode A: FDD Mode B: FDD/TDD TDMA+DAMA (u) TDM/TDMA (d)</td>
</tr>
<tr>
<td>Channelisation schemes</td>
<td>28 MHz (u/d)</td>
<td>20-40 MHz (u/d) or 25-50 MHz(u/d)</td>
</tr>
<tr>
<td></td>
<td>possibility for 14 MHz (u)</td>
<td>no smaller channels to avoid higher order modulations</td>
</tr>
<tr>
<td>Recommended modulations</td>
<td>4/16-QAM + 64-QAM as option (d) 4-QAM + 16-QAM as option (u)</td>
<td>Mode A (FDD): QPSK + 16-QAM as option Mode B (FDD/TDD): QPSK/16-QAM + 64-QAM as option</td>
</tr>
<tr>
<td>Capacity</td>
<td>60 Mb/s (d) 30 Mb/s (u)</td>
<td>16, 20, 32, 40 Mbauds for 20, 25, 40 and 50 MHz channels, respectively.</td>
</tr>
<tr>
<td></td>
<td>Symmetrical capability although instantaneous traffic need not be symmetrical</td>
<td></td>
</tr>
</tbody>
</table>
IEEE802.16 WirelessMAN

802.16 Features

• LMDS in 10 - 66GHz band
• Point to Multipoint
• Big block sizes
• Air Interface designated “WirelessMAN-SC”
  – SC = Single Carrier Modulation
    • Usually QPSK 32 QAM
    • No OFDM
• Uplink Access by Time Division Multiple Access (TDMA)
• Burst design allows both Time Division Duplex (TDD) and Frequency Division Duplex (FDD)
• Adaptive Burst Profiles allow modulation and cosing to be assigned dynamically on a burst-by-burst basis
802.16a Features

- MMDS (Task Group 3)
  - Non-Line of Sight
- 6MHz bandwidth in 2 - 11GHZ band
- 10ms latency requirement
- 3 Modulation schemes
  - WirelessMAN-SC2
    - Single Carrier modulation
  - WirelessMAN-OFDM
    - OFDM with 256-point FFT
    - TDMA access
  - WirelessMAN-OFDMA
    - OFDM with 2048-point FFT
    - Multiple carriers are assigned to multiple receivers to address multiple access requirements
802.16b Features

• UNI2 (Task Group 4)
• Unlicensed band (5 - 6GHz) with 20MHz bandwidth
• Lower power specification
• OFDM and Adaptive Modulation QAM
FPGA complexity rises to meet Broadbands requirements

- Analog
- Proprietary
- 802.16 HiperAccess

Device Complexity

1985: XC2000-XC3000
1992: XC4000, Virtex
2000: Virtex-II
2002: Virtex-II Pro
2004: Platform For Programmable Systems

- PowerPC
- RocketIO

- Glue Logic
- System-Level Function Blocks
  - DLLs
  - High Perf. IO
  - Block RAM
  - Distributed Memory
- Platform FPGAs
  - IP Immersion
  - 840 Mbps LVDS
  - TripleDES
  - XCITE
  - Multiplier
  - DCM
Performance Limitation of Conventional DSP Chips

- Fixed inflexible architecture
  - Typically 1-4 MAC units
  - Fixed data width
- Serial processing limits data throughput
  - Time-shared MAC unit
  - High clock frequency creates difficult system-challenge

Example
256 Tap FIR Filter = 256 multiply and accumulate (MAC) operations per data sample
Performance Advantage of FPGAs

- Flexible architecture
  - Distributed DSP resources (LUT, registers, multipliers, & memory)
- Parallel processing maximizes data throughput
  - Support any level of parallelism
  - Optimal performance/cost tradeoff
- FPGAs also support serial processing

Example
256 Tap FIR Filter = 256 multiply and accumulate (MAC) operations per data sample
Broadband Fixed Wireless Infrastructure

• Basestations
  – Similar functional blocks to mobile cellular systems
  – Base-band processing of signals from multiple channels
  – Modulation/Demodulation
  – Pulse-Shape Filtering & other high-speed signal processing

• Backbone Network Gateway
  – Interface cards from basestation to wired network
  – Packet segmentation, assembly and routing
FPGAs in Broadband Wireless Basestations

• Very high-speed signal processing
  – Many channels can be processed at once
  – Much higher speed than single DSP processors can achieve
  – More cost effective than DSP “farms”

• Forward Error Correction
  – Multiple Channels
  – Reed-Solomon, Viterbi, Turbo Convolutional and Turbo Product Codes available.
FPGAs in Broadband Wireless Basestations

• Control and Bridging functions
  – Connecting ASSPs, ASICs, Processors and Memory together

• Adaptable interfaces to different backbone network standards
  – Minimize system design changes to allow products to fit with many different networking standards and protocols
FPGAs in Broadband Wireless Basestations

• Backplane
  – Backplanes in basestations are usually proprietary
    • LVDS signalling is common
      – There are many Xilinx FPGAs, large and small, with LVDS I/O capability
  – New move to standardize on Gigabit Serial I/O
    • PICMIG 3.x: Still being discussed
  – Some projections estimate 30% of electronic portion of basestation cost to be due to backplane
    • Drives the need to standardize and move to Gigabit serial
Broadband Wireless Network Terminals

- Most Broadband Fixed Wireless terminal stations are mains powered
  - Reduced requirement for ultra low-power
- Volumes lower than for cellular mobiles
  - Market requirements and expected volumes make ASIC/ASSP development more of a risk
- Changing markets provide new opportunities to companies to establish market leadership
  - Early product introduction
Broadband Wireless Network Terminals

- Many possible variants for a wide range of different end-users around the world
  - Programmable Logic flexibility enables a common set of cards to be developed that can address many different markets & standards
- Programmable Logic enables early support of new and emerging wireless and wired standards
  - Terminals acting as gateways between Broadband Fixed Wireless and Home Networking Standards
    - W-LAN, Bluetooth, Powerline,
Xilinx in Broadband Fixed Wireless Network Terminals

- Filtering, Demodulation, Pre-Distortion
- Forward Error Correction schemes
- Encryption/De-cryption
- Multi-channel data stream multiplexing/demultiplexing
- ASSP interfacing and control
  - Coolrunner and Spartan-II/E ideal for interfacing to and controlling ASSPs that may have been developed initially for related technologies such as WirelessLAN & Bluetooth
WirelessMAN
Adaptive Modulation

• Modulation and FEC are dynamically assigned according to link conditions
• Burst-by-burst, per subscriber station
• Trade-off capacity vs. robustness in real time
• Approximately doubles capacity for a given cell area
Baud Rates & Channel Size (10-66 GHz GHz)

- Enables equipment manufactures to choose according to spectrum requirements

<table>
<thead>
<tr>
<th>Channel Width (MHz)</th>
<th>Symbol Rate (Msym/s)</th>
<th>QPSK Bit Rate</th>
<th>16-QAM Bit Rate</th>
<th>64-QAM Bit Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>16</td>
<td>32</td>
<td>64</td>
<td>96</td>
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<tr>
<td>25</td>
<td>20</td>
<td>40</td>
<td>80</td>
<td>120</td>
</tr>
<tr>
<td>28</td>
<td>22.4</td>
<td>44.8</td>
<td>89.6</td>
<td>134.4</td>
</tr>
</tbody>
</table>
802.16 TDD Frame

\[ n \text{ PS} = \frac{(\text{Symbol Rate} \times \text{Frame Length})}{4} \]

Downlink Subframe

Adaptive

Uplink Subframe
WirelessMAN
Downlink Framing

FDD Mode Example

- Downlink MAP specifies
  - Modulation and FEC changes required for each TDM portion
  - Data is transmitted in order of decreasing robustness

- In FDD systems TDM followed by TDMA segment
  - Each has new preamble at start of burst profile to allow better support of half-duplex subscriber stations (SS)
WirelessMAN
Uplink Sub-Frame

Initial maintenance opportunities (UIUC = 2)
Request contention opps (UIUC = 1)
SS 1 scheduled data (UIUC = j)

SS transition gap
Tx/Rx transition gap (TDD)

Access burst
Collision
Access burst
Bandwidth request
Collision
Bandwidth request

Access burst
Collision
Access burst
Bandwidth request
Collision
Bandwidth request

SS N scheduled data (UIUC = j)
802.16 MAC

- Connection-oriented
- Works in difficult user environments
  - High bandwidth, hundreds of users per channel
  - Continuous and burst traffic
  - Efficient use of spectrum
- Protocol-Independent
  - (ATM, IP, Ethernet, ...)
- Flexible QoS
  - CBR, CBR, rt rt-VBR, -VBR, nrt nrt-VBR, BE, with granularity within classes
- Supports multiple 802.16 PHYs
MAC Addressing

• Subscriber Station (SS) has 48-bit IEEE MAC Address
• Base-Station (BS) has 48-bit Base Station ID
  – 24-bit operator indicator
  – Not a MAC address
• 16-bit Connection ID (CID)
  – Used in MAC Protocol Data Units
Transmission of PDU

MAC Message

SDU 1       SDU 2

MAC PDUs

PDU 1       PDU 2       PDU 3       PDU 4       PDU 5

Burst

P       FEC 1       FEC 2       FEC 3

FEC Blocks

Preamble
IEEE 802.16a Compliant
Viterbi Decoder Feature Set

- Reaches OC3 (155Mbps) data rates and higher
- Parallel radix-2 architecture for high speed and compact size
- Soft decision input data with parameterizable width
- Industry-standard constraint length 7, G0=171, G1=133
- Zero-Tail termination circuitry to reduce latency requirements
- Traceback length 48 or 96 for two clock version
- Traceback length up to 127 for the one-clock version
- Normalization output
- Erasure capability to improve BER
- VHDL source code distribution
Xilinx IEEE 802-Compatible Viterbi Decoder

- Resources and performance table

<table>
<thead>
<tr>
<th>Design</th>
<th>Viterbi2x</th>
<th>Viterbi1x</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traceback Length</td>
<td>48</td>
<td>96</td>
</tr>
<tr>
<td>Soft Data Width</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Area (Slices)</td>
<td>1084</td>
<td>1084</td>
</tr>
<tr>
<td>Area/No BSC</td>
<td>897</td>
<td>897</td>
</tr>
<tr>
<td>Block RAM</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Continuous Latency</td>
<td>162</td>
<td>306</td>
</tr>
<tr>
<td>Tail-Bite Latency</td>
<td>113</td>
<td>209</td>
</tr>
<tr>
<td>Zero-Tail Latency</td>
<td>65</td>
<td>113</td>
</tr>
<tr>
<td>Maximum Clock Frequency (MHz)</td>
<td>157</td>
<td>157</td>
</tr>
</tbody>
</table>

Latency Improvement through use of Zero-Tail Termination
Turbo Product Encoder

- Performs TPC encoding as defined in the IEEE 802.16 and 802.16a standards
- Block sizes from 64 bits to 4 Kbits, 64 possible product codes
- Up to 8 Kbits of internal buffering
- Low latency (13 clocks) independent of code type
- VHDL Source Code distribution synthesizable with Synplify Pro
- Incorporates Xilinx Smart-IP Technology for maximum and predictable
Turbo Product Decoder

- Conforms to turbo product specification listed in the IEEE 802.16 and 802.16a standards
  - Based on the Comtech AHA Corporation (AHA) TPC Galaxy Core
- Block sizes from 64 bits to 4 Kbits, 64 product codes
- Data rate > 155 Mbps
  - with five iterations using (64,57)2 code
- Provides up to 10 dB of coding gain over Reed-Solomon concatenated with Viterbi in an MMDS fading channel at a BER of 10-6
- Uses Xilinx Smart-IP Technology
Bit Error Rate (BER) performance versus Viterbi & Uncoded BPSK
Xilinx Turbo Product Codec
Performance & Utilization

- Size and clock speed
- Maximum Data Rates shown for a subset of codes and by number of iterations

<table>
<thead>
<tr>
<th>Turbo Product</th>
<th>I/O</th>
<th>Slices</th>
<th>Block RAMS</th>
<th>Max. Clk Virtex-II</th>
<th>Max. Clk Virtex-II Pro</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPC Encoder</td>
<td>17</td>
<td>80</td>
<td>2</td>
<td>285 MHz</td>
<td>340 MHz</td>
</tr>
<tr>
<td>TPC Decoder</td>
<td>75</td>
<td>3313</td>
<td>17</td>
<td>150 MHz</td>
<td>170 MHz</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Code Type</th>
<th>Code Rate</th>
<th>Number of Iterations</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>x</td>
<td>y</td>
</tr>
<tr>
<td>(64,57)</td>
<td>(64,57)</td>
<td>0.793</td>
</tr>
<tr>
<td>(64,57)</td>
<td>(32,31)</td>
<td>0.863</td>
</tr>
<tr>
<td>(64,57)</td>
<td>(32,26)</td>
<td>0.724</td>
</tr>
<tr>
<td>(64,57)</td>
<td>(16,15)</td>
<td>0.835</td>
</tr>
<tr>
<td>(32,26)</td>
<td>(32,26)</td>
<td>0.660</td>
</tr>
<tr>
<td>(64,57)</td>
<td>(8,7)</td>
<td>0.779</td>
</tr>
<tr>
<td>(32,26)</td>
<td>(16,11)</td>
<td>0.559</td>
</tr>
<tr>
<td>(16,11)</td>
<td>(16,11)</td>
<td>0.473</td>
</tr>
</tbody>
</table>
Virtex-II Pro FPGA
Platform for Programmable Systems

- Industry’s Fastest FPGA Fabric
- Up to 4 IBM PowerPC™ Processors immersed in FPGA Fabric
- Up to 24 Embedded Rocket I/O™ Multi-Gigabit Transceivers
- Up to 12 Digital Clock Managers
- XCITE Digitally Controlled Impedance Technology
- Up to 556 18x18 Multipliers
- Over 10 Mb Embedded Block RAM
Virtex-II Series Expanded to Include Virtex-II Pro

- Virtex-II Logic, Routing, Features
  - Upward compatible, same design tools
  - Embedded Multipliers, SelectIO-Ultra (with 840Mbps LVDS), DCI/XCITE, DCM

- Up to 16, 3.125 Gbps serial transceivers
  - Channel bonding, 8b/10b encoding
  - Supports high-speed interfaces GbE, 10GbE (XAUI), PCI/PCI-X, Infiniband, RapidIO, HyperTransport, FlexBus 3/4, POS-PHY 3/4

- Up to four IBM 405 PowerPC®
  - 32-bit RISC CPU: 450 DMIPS @ 300 MHz
  - The leading embedded CPU architecture in telecom & networking infrastructure
  - IBM CoreConnect™ on-chip bus
  - MicroBlaze SoftProcessors can also be used alongside
Virtex-II Pro Enables Transition from Parallel to Serial I/Fs

- 25 I/O Standards
- XCITE Technology
- 840 Mbps LVDS
- Dedicated DDR Registers

- Helps preserve investment in legacy designs
- Eases transition from parallel to serial technology
- Parallel interface designs will not go away

Rocket I/O Multi-Gigabit Serial Transceivers
Up to Twenty Four 3.125 Gbps transceivers

Gb Serial Transceiver

32b @ 78 MHz

Gb Serial Transceiver

32b @ 78 MHz

GB

PAD

Reg

Reg

Reg

Reg

Reg

3-State

DDR mux

DDR mux

Output

Input

IOB

IOB

F

N

DDR FF

Reg

Reg

Reg

Reg
## The Virtex-II Pro Family

<table>
<thead>
<tr>
<th>Device</th>
<th>2VP2</th>
<th>2VP4</th>
<th>2VP7</th>
<th>2VP20</th>
<th>2VP30</th>
<th>2VP40</th>
<th>2VP50</th>
<th>2VP70</th>
<th>2VP100</th>
<th>2VP125</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells</td>
<td>3,168</td>
<td>6,768</td>
<td>11,088</td>
<td>20,880</td>
<td>30,816</td>
<td>43,632</td>
<td>53,136</td>
<td>74,448</td>
<td>99,216</td>
<td>125,136</td>
</tr>
<tr>
<td>Block RAM (Kbits)</td>
<td>216</td>
<td>504</td>
<td>792</td>
<td>1,584</td>
<td>2,448</td>
<td>3,456</td>
<td>4,176</td>
<td>5,904</td>
<td>7,992</td>
<td>10,008</td>
</tr>
<tr>
<td>18 x18 Multipliers</td>
<td>12</td>
<td>28</td>
<td>44</td>
<td>88</td>
<td>136</td>
<td>192</td>
<td>232</td>
<td>328</td>
<td>444</td>
<td>556</td>
</tr>
<tr>
<td>Digital Clock Management Blocks</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>Configuration Memory (Mbits)</td>
<td>1.31</td>
<td>3.01</td>
<td>4.49</td>
<td>8.21</td>
<td>11.36</td>
<td>15.56</td>
<td>19.02</td>
<td>25.6</td>
<td>33.65</td>
<td>42.78</td>
</tr>
<tr>
<td>IBM PowerPC Processors</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Rocket I/O Multi-Gigabit Transceivers</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>12*</td>
<td>16*</td>
<td>20</td>
<td>20*</td>
<td>24*</td>
</tr>
<tr>
<td>Max Available User I/O</td>
<td>204</td>
<td>348</td>
<td>396</td>
<td>564</td>
<td>692</td>
<td>804</td>
<td>852</td>
<td>996</td>
<td>1164</td>
<td>1200</td>
</tr>
</tbody>
</table>

### Package

<table>
<thead>
<tr>
<th>Package</th>
<th>FG256</th>
<th>FG456</th>
<th>FF672</th>
<th>FF896</th>
<th>FF1152</th>
<th>FF1148</th>
<th>FF1517</th>
<th>FF1704</th>
<th>FF1696</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>140</td>
<td>140</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td></td>
<td>156</td>
<td>248</td>
<td>248</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td>204</td>
<td>348</td>
<td>396</td>
<td>556</td>
<td>956</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>396</td>
<td>556</td>
<td>556</td>
<td>692</td>
<td>812*</td>
<td>964</td>
</tr>
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<td>564</td>
<td>692</td>
<td>692</td>
<td>692</td>
<td>804*</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>804*</td>
<td>812*</td>
<td>812*</td>
<td>852</td>
</tr>
<tr>
<td></td>
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<td>956</td>
<td></td>
<td></td>
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<td>1164*</td>
<td>1200*</td>
</tr>
</tbody>
</table>

*Note: FF1148 and FF1696 packages support higher user I/O and zero Rocket I/O Multi-Gigabit Transceivers*
Virtex-II Platform FPGA
The Winning Architecture

- #1 FPGA architecture
- 150 nm 8-layer metal CMOS
- Advanced logic & routing
- Highest density in the industry
- Embedded Dual Port RAM

- BlockRAM
- XtremeDSP™ - multipliers
- DCM™
- XCITE technology - DCI
- SelectIO-Ultra™
- Triple DES security
- IP-Immersion™ technology
Virtex-II Features

- Embedded DSP functionality - up to 500 Billion MAC/s
- Embedded Dual-Port RAM - for Data Buffering
- XCITE Digitally-Controlled Impedance (DCI) for simpler PCB layout
- Digital Clock Management (DCM) - Precise Clock Generation
- Active Interconnect Technology with a 300 MHz System Clock
- SelectIO™ 25 IO types including 840 Mbps LVDS
## The Virtex-II Family

<table>
<thead>
<tr>
<th>Virtex-II Part Number</th>
<th>XC2V40</th>
<th>XC2V80</th>
<th>XC2V250</th>
<th>XC2V500</th>
<th>XC2V1000</th>
<th>XC2V1500</th>
<th>XC2V2000</th>
<th>XC2V3000</th>
<th>XC2V4000</th>
<th>XC2V6000</th>
<th>XC2V8000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells</td>
<td>576</td>
<td>1152</td>
<td>3456</td>
<td>6912</td>
<td>11520</td>
<td>17280</td>
<td>24192</td>
<td>32256</td>
<td>51840</td>
<td>76032</td>
<td>104832</td>
</tr>
<tr>
<td>BRAM (Kb)</td>
<td>72</td>
<td>144</td>
<td>432</td>
<td>576</td>
<td>720</td>
<td>864</td>
<td>1008</td>
<td>1728</td>
<td>2160</td>
<td>2592</td>
<td>3024</td>
</tr>
<tr>
<td>Multipliers</td>
<td>4</td>
<td>8</td>
<td>24</td>
<td>32</td>
<td>40</td>
<td>48</td>
<td>68</td>
<td>96</td>
<td>120</td>
<td>144</td>
<td>168</td>
</tr>
<tr>
<td>DCM Units</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>FG256</td>
<td>88</td>
<td>120</td>
<td>172</td>
<td>172</td>
<td>172</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FG456</td>
<td>200</td>
<td>264</td>
<td>324</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FG676</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>392</td>
<td>456</td>
<td>484</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF896</td>
<td>432</td>
<td>528</td>
<td>624</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF1152</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF1517</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>912</td>
<td>1104</td>
</tr>
<tr>
<td>BG575</td>
<td>328</td>
<td>392</td>
<td>408</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BG728</td>
<td></td>
<td></td>
<td></td>
<td>456</td>
<td>516</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BF957</td>
<td>624</td>
<td>684</td>
<td>684</td>
<td>684</td>
<td>684</td>
<td>684</td>
<td>684</td>
<td>684</td>
<td>684</td>
<td>684</td>
<td>684</td>
</tr>
</tbody>
</table>

11 Devices, 10 Packages, 34 combinations
Low Cost Spartan-IIIE FPGA
Total Cost Management for Consumer Products

- Hardware software co-development
- Fewer engineering man hours
- No NRE charges

- No obsolete inventory
- Extend product life through design upgrades

- Cost-optimized silicon and packaging
- System features reduce discrete parts on boards
- Stock one part for many applications
## Spartan-IIE Family at a Glance

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Voltage</td>
<td>1.8 Volts</td>
</tr>
<tr>
<td>Architecture</td>
<td>Virtex-E Based</td>
</tr>
<tr>
<td>5V Tolerant I/O</td>
<td>Yes*</td>
</tr>
<tr>
<td>I/O Performance</td>
<td>&gt;300 MHz</td>
</tr>
<tr>
<td>Differential I/O Performance</td>
<td>Up to 400 Mbps</td>
</tr>
<tr>
<td>I/O Standards Supported</td>
<td>19 standards</td>
</tr>
<tr>
<td></td>
<td>(including LVDS, BLVDS, and LVPECL)</td>
</tr>
<tr>
<td>DLL's</td>
<td>4</td>
</tr>
<tr>
<td>Memory</td>
<td>Distributed RAM + Block RAM</td>
</tr>
<tr>
<td>Densities</td>
<td>50K – 300K system gates</td>
</tr>
<tr>
<td>Speed Grades</td>
<td>-6 and –7</td>
</tr>
<tr>
<td>Packages</td>
<td>TQ144, PQ208, FT256, FG456</td>
</tr>
</tbody>
</table>

* When a series resistor is used
Spartan-IIIE Capabilities

- **Flexible Clocking**
  - Delay Locked Loops (DLL): clock multiply, divide, de-skew, and phase shift

- **On-chip Memory**
  - Parameterizable block RAM and distributed RAM

- **Advanced Interfacing**
  - Support for 19 I/O standards:
    - **Chip to Backplane**: PCI, GTL, GTL+, AGP 2X
    - **Chip to Memory**: HSTL-I, HSTL-III, HSTL-IV, SSTL3-I, SSTL3-II, SSTL2-I, SSTL2-II, CTT
    - **Chip to Chip**: LV TTL, LVCMOS2/18
    - **Differential**: LVDS, BusLVDS, LVPECL

- **Cost-optimized DSP**
  - Nearly one billions MAC/s/$
  - System Generator tool bridges directly to MathWorks DSP tool suite
  - Reed Solomon, Viterbi Decoder, Convolution Encoder, Interleaver/De-interleaver, Color Space Converters, Other DSP building blocks

- **Soft Processors and Other IP**
  - Over 200 algorithms and cores
    - Interfacing: Cardbus, Ethernet, POS-PHY 3
    - Processors: MicroBlaze, PicoBlaze CoreConnect, ARC
    - General purpose: CAM, FIFOs, memory
Spartan-IIE - System Integration

Spartan-IIE system features eliminate the need for many discrete components.
Discrete cost savings can more than pay for the FPGA itself.
## Xilinx CPLD Devices

<table>
<thead>
<tr>
<th>Feature</th>
<th>CoolRunner-II</th>
<th>XPLA3</th>
<th>9500XL/XV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Voltage</td>
<td>1.8</td>
<td>3.3</td>
<td>3.3/2.5</td>
</tr>
<tr>
<td>Low Power</td>
<td>FZP plus DataGATE</td>
<td>FZP</td>
<td>Low power mode</td>
</tr>
<tr>
<td>Global Clock</td>
<td>3</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>P-Term Inputs</td>
<td>40</td>
<td>40</td>
<td>54</td>
</tr>
<tr>
<td>Clock Management</td>
<td>Divide, Doubler &amp; CoolCLOCK</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>I/O Standards</td>
<td>LVTTL, LVCMOS, HSTL, SSTL</td>
<td>LVTTL, LVCMOS</td>
<td>LVTTL, LVCMOS</td>
</tr>
<tr>
<td>I/O Banks</td>
<td>1 to 4</td>
<td>1</td>
<td>1 to 4 (XV), 1 (XL)</td>
</tr>
<tr>
<td>Macrocells</td>
<td>32-512</td>
<td>32-512</td>
<td>36-288</td>
</tr>
<tr>
<td>tPD / Fmax</td>
<td>3.5 / 303</td>
<td>5 / 200</td>
<td>4.0 / 250</td>
</tr>
<tr>
<td>Security</td>
<td>Multiple levels</td>
<td>1 level</td>
<td>1 level</td>
</tr>
<tr>
<td>Process Technology</td>
<td>0.18u</td>
<td>0.35u</td>
<td>0.35u / 0.25u</td>
</tr>
</tbody>
</table>
Key Xilinx Value Propositions

• Market moving from proprietary architectures to ones based on international standards
  – Requires flexibility and Time-to-Market
  – Manufacturers looking to modify or provide upgrade paths for their current equipment

• FPGA technology is key to maximum hardware flexibility
  – Design can be changed throughout the product development cycle
Key Xilinx Value Propositions

- XtremeDSP
  - High-speed processing to be performed in the transmitter and receiver
  - Helps reduce $’s per channel
    - As many channels as possible need to be processed by a single chip
    - DSPs cannot meet the requires performance criteria
  - Very high performance Error Correction
    - Offload high performance tasks from the systems DSP or Microprocessor
Key Xilinx Value Propositions

- In Field Reconfiguration and Test
  - Many towers will be deployed in remote locations so the ability to change a design in-field is highly desirable
    - Meet changing specifications
    - Bug fixes
    - Solve equipment compatibility problems
    - Add new features
    - Remote system testing and diagnostics

Extended Window of Innovation

Revenue

Time to Market Advantage

Field Upgrade Advantage with Xilinx Online

Fixed Chip Solution

Time
Xilinx IP/Core?
Time-to-Market Advantage

ASIC Design Cycle

FPGA Design Cycle
Reduce design implementation / verification time.

IP / Cores
Complex Designs Optimized and Verified.
Reduce Implementation, & Customization time.

System Platforms: e.g Prototyping boards further reduce design time.
Key IP for Fixed Wireless Solutions

• High Speed (>155Mbps) Viterbi
  – Soft decision input data with parameterizable width
  – Industry-standard constraint length 7, G0=171, G1=133
  – Traceback length up to 127 for the one-clock version
  – Supports puncturing through an external interface
  – Bit Error Rate (BER) monitor through an external circuit
  – Best State feature in traceback improves BER by up to 0.2 dB compared to Qualcomm Q1900
  – Erasure capability to improve BER

Key IP for Fixed Wireless Solutions

• FFT/iFFT
  – At the heart of OFDM systems, such as those used in BFWA networks

• FEC Solutions
  – Reed Solomon
  – Turbo Product Codecs
  – Turbo Convolutional Codecs

• Filters
  – Used for Pulse Shaping, Pre-distortion

• Digital Down Conversion

• NCOs, Sin/Cos Look-Up Tables, Multipliers...
• Keep up to date with the latest cores and reference designs available from Xilinx and our AllianceCore partners
System Generator for DSP

- Visual data flow paradigm
- Polymorphic block libraries
- Bit and cycle true modeling
- Seamlessly integrated with Simulink and MATLAB
  - Test bench and data analysis
- Automatic code generation
  - Synthesizable VHDL
  - IP cores
  - HDL test bench
  - Project and constraint files
Xilinx Design Services Expertise

• Design case studies and evaluations can be undertaken for customers
• Xilinx Design Services have already done designs for W-CDMA base-band processing, SDH Microwave Links and numerous network equipment
• Can offer software and hardware support/development for the customer
ITU-T J.83 Req QAM 128 Modulator

QAM 128 Modulator for SDH Wireless Radio: Point-to-Point
ITU-T J.83 Req QAM 128 Modulator

- Point-to-Point SDH Data wireless system
- XDS Design Study proposed implementation of 4 Tx path modulators guaranteeing 121MHz operation
- Each channel included Error Correction, Filtering & Modulation
  - Advanced system partitioning used to achieve the density
- Design size reduced by 90% from non-optimised architecture
  - Device used XCV400E-5BG676
- Code delivered allowed customer to re-synthesize variations made to filter & modulation parameters during system test

Contact Xilinx Design Services for more details
Summary

• Xilinx devices fit perfectly in the Broadband Fixed Wireless Market
  – High Speed Signal Processing
  – Flexible Logic design

• Market is undergoing radical changes, with the introduction of international standards, so maintaining flexibility is crucial
  – FPGAs allow rapid Time-To-Market, and extend a product’s Time-In-Market
  – Proprietary systems & protocols will still need to be supported
  – Specifications have only just been completed and are liable to changes and new revisions
More Information


Questions?

espteam@xilinx.com