Entering the Era of “Crossover” SoCs

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A crossover is a vehicle built on a car platform and combining, in highly variable degrees, features of a traditional sport utility SUV with features from a passenger vehicle.
A New SoC Implementation Category

- **ASICS**: Higher Development Cost, Limited Flexibility, Lower Unit Cost
- **ASSP**: Crossover Spectrum
- **X-SoC**: Higher Flexibility, Higher Unit Cost
- **FPGAs**
Driving the need for Crossover SoCs

Market Forces
- High Flexibility
- TTM
- Cost

Crossover SoC
- Application Focus
- Development Cost
- Financial Constraints
- Technology Innovation
- High Integration

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Definition of SoC

- The integration of (nearly) all necessary electronic functions of a system in one package
- Characterized by high bandwidth and low latency integration of
  - Programmable processors
  - Accelerator units
  - Memories
  - IO functions
- Software programmable
Historical Approaches
The Evolution of FPGAs
Riding Moore’s Law

- **Programmable**
  - Programmable switches and functions

- **Parallelism**
  - Performance and power

- **Distributed memory**
  - High BW memory

- **Regular**
  - Manufacturable

- **Scalable**
  - Future proof

+ PCI-e, Ethernet, DSPs, MGTs
+ Soft Processors, DSP functions

2.4 TeraMac/s
2.8 Tera Bps BW
2M Logic Cells
100Mbit Memory

Programmable
*Gate Arrays*
Structured ASIC

- Lower cost
- No programmability
- Heterogeneous integration
- Substrate limits metal density
- Minimum pitch \( \geq 125 \) microns
- Limits die connectivity
- Limits BW and latency
- Wastes power
Enabling the Next Wave of Crossover SOCs

Monolithic
CPU + Programmable Logic

3D System in Package

Package

CPU
Mem
Prog. Logic.
Embedded Processing Subsystem: Tightening The CPU–FPGA Connection

Progression towards higher bandwidth, lower latency and ease of use

**IO extension**
- CPU
- Northbridge
- Southbridge
- FPGA

**Acceleration**
- CPU
- Southbridge
- FPGA

**Co-processing**
- CPU
- FPGA

**Peer Processing**
- CPU
- FPGA
- NOC
Blending of CPU and Programmable Logic

Processing System
- Common Peripherals
- High-Bandwidth Interfaces

Memory Interfaces

Dual Core Processor
- Cache
- Cache

High-Bandwidth Interfaces

Accelerators

IO Peripherals

Programmable Logic

High Bandwidth
Low Latency

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X-SoC: Seamless Integration CPU - FPGA
Heterogenous Multi-core
Evolution Towards 3D SoCs

Traditional MCM

Silicon Interposer
“2.5 D”

3D

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Integration of Heterogeneous Technologies

2.5D- Active on Passive
- Side-by-side die placement
- Active
- Passive

3D- Active on Active
- Vertical die stacking
- Active

PCB

Interposer

FPGA

RAM

Logic

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“More than Moore”
Enables High Bandwidth, Low Power Connectivity

100X bandwidth / Watt advantage over conventional methods

Stacked Silicon Interconnect

SerDes & Standard I/O

100X band-to-Chip I/O Count

10X

1X

10X

100X

1000X

BW / Watt
The Need to Develop and Evolve Standards

- **CPU- FPGA Interconnect**
  - Signal Interconnect : e.g. AXI
  - Data Transfer Protocols : e.g. MCAPI

- **3D Interconnect**
  - Design Enablement
    - Models
    - 3D Process Development Kit
  - Manufacturing standards
    - DFM rules for TSV, microbump
  - Interoperability of silicon
New Crossover Business Models Will Emerge

- SoC platform providers
- Silicon slice suppliers
- New breed of “chipless” ASSP startups
Conclusion

The age of crossovers has begun!

- IC landscape will change dramatically
- Heterogeneous multi-core and 3D are key
- Standards are key enablers