

CORE Generator Update Installer Guide



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5,748,979; 5,752,006; 5,752,035; 5,754,459; 5,758,192; 5,760,603; 5,760,604; 5,760,607; 5,761,483; 5,764,076; 5,764,534; 5,764,564; 5,768,179; 5,770,951; 5,773,993; 5,778,439; 5,781,756; 5,784,313; 5,784,577; 5,786,240; 5,787,007; 5,789,938; 5,790,479; 5,790,882; 5,795,068; 5,796,269; 5,798,656; 5,801,546; 5,801,547; 5,801,548; 5,808,479; 5,811,985; 5,815,004; 5,815,016; 5,815,404; 5,815,405; 5,818,255; 5,818,730; 5,821,772; 5,821,774; 5,825,202; 5,825,662; 5,825,787; 5,828,230; 5,828,231; 5,828,236; 5,828,608; 5,831,448; 5,831,460; 5,831,845; 5,831,907; 5,835,402; 5,838,167; 5,838,901; 5,838,954; 5,841,296; 5,841,867; 5,844,422; 5,844,424; 5,844,829; 5,844,844; 5,847,577; 5,847,579; 5,847,580; 5,847,993; 5,852,323; 5,861,761; 5,862,082; 5,867,396; 5,870,309; 5,870,327; 5,870,586; 5,874,834; 5,875,111; 5,877,632; 5,877,979; 5,880,492; 5,880,598; 5,880,620; 5,883,525; 5,883,852; 5,886,538; 5,889,411; 5,889,412; 5,889,413; 5,889,701; 5,892,681; 5,892,961; 5,894,420; 5,896,047; 5,896,329; 5,898,319; 5,898,320; 5,898,602; 5,898,618; 5,898,893; 5,907,245; 5,907,248; 5,909,125; 5,909,453; 5,910,732; 5,912,937; 5,914,514; 5,914,616; 5,920,201; 5,920,202; 5,920,223; 5,923,185; 5,923,602; 5,923,614; 5,928,338; 5,931,962; 5,933,023; 5,933,025; 5,933,369; 5,936,415; 5,936,424; 5,939,930; 5,940,606; 5,942,913; 5,944,813; 5,945,837; 5,946,478; 5,949,690; 5,949,712; 5,949,983; 5,949,987; 5,952,839; 5,952,846; 5,955,888; 5,956,748; 5,958,026; 5,959,821; 5,959,881; 5,959,885; 5,961,576; 5,962,881; 5,963,048; 5,963,050; 5,969,539; 5,969,543; 5,970,142; 5,970,372; 5,971,595; 5,973,506; 5,978,260; 5,986,958; 5,990,704; 5,991,523; 5,991,788; 5,991,880; 5,991,908; 5,995,419; 5,995,744; 5,995,988; 5,999,014; 5,999,025; 6,002,268; 6,002,282; 6,002,991; 6,005,423; 6,005,829; 6,008,666; 6,011,407; 6,011,740; 6,016,063; 6,018,250; 6,018,624; 6,020,633; 6,020,756; 6,020,757; 6,020,776; 6,021,423; 6,023,564; 6,023,565; 6,025,736; 6,026,481; 6,028,445; 6,028,450; 6,033,938; 6,034,542; 6,034,548; 6,034,557; 6,035,106; 6,037,800; 6,038,386; 6,041,340; 6,043,692; 6,044,012; 6,044,025; 6,046,603; 6,047,115; 6,049,222; 6,049,227; 6,051,992; 6,054,871; 6,055,205; 6,057,589; 6,057,704; 6,057,708; 6,061,417; 6,061,418; 6,067,508; 6,069,488; 6,069,489; 6,069,490; 6,069,849; 6,070,260; 6,071,314; 6,072,348; 6,073,154; 6,074,432; 6,075,418; 6,078,201; 6,078,209; 6,078,528; 6,078,735; 6,078,736; 6,081,914; 6,084,429; 6,086,629; 6,086,631; 6,091,262; 6,091,263; 6,091,892; 6,094,063; 6,094,065; 6,094,385; 6,097,210; 6,097,238; 6,099,583; 6,100,705; 6,101,132; 6,101,143; 6,104,211; 6,105,105; 6,107,821; 6,107,826; 6,107,827; 6,112,322; 6,114,843; 6,118,286; 6,118,298; 6,118,300; 6,118,324; 6,118,869; 6,118,938; 6,120,549; 6,120,551; 6,121,795; 6,124,724; 6,124,731; 6,130,550; 6,133,751; 6,134,191; 6,134,517; 6,137,307; 6,137,714; 6,144,220; 6,144,225; 6,144,262; 6,144,933; 6,150,838; 6,150,839; 6,150,863; 6,154,048; 6,154,049; 6,154,052; 6,154,053; 6,157,209; 6,157,211; 6,157,213; 6,160,418; 6,160,431; 6,163,167; 6,167,001; 6,167,416; 6,167,545; 6,167,558; 6,167,560; 6,172,518; 6,172,519; 6,172,520; 6,173,241; 6,175,246; 6,175,530; 6,177,819; 6,177,830; 6,181,158; 6,181,164; 6,184,708; 6,184,709; 6,184,712; 6,185,724; 6,188,091; 6,191,610; 6,191,613; 6,191,614; 6,192,436; 6,195,774; 6,199,192; 6,201,406; 6,201,410; 6,201,411; and 6,202,106; Re. 34,363, Re. 34,444, and Re. 34,808. Other U.S. and foreign patents pending. Xilinx, Inc. does not represent that devices shown or products described herein are free from patent infringement or from any other third party right. Xilinx, Inc. assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction if such be made. Xilinx, Inc. will not assume any liability for the accuracy or correctness of any engineering or software support or assistance provided to a user.

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About This Manual

Manual Contents

This book contains the following chapters.

- “Introduction” chapter
- “Getting Started” chapter
- “CORE Generator Update Installer Tool” chapter

Additional Resources

For additional information, go to <http://support.xilinx.com>. The following table lists some of the resources you can access from this Web site. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answers Database	Current listing of solution records for the Xilinx software tools Search this database using the search function at http://support.xilinx.com/support/searchtd.htm
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm

Resource	Description/URL
Data Book	Pages from <i>The Programmable Logic Data Book</i> , which contains device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging http://support.xilinx.com/partinfo/databook.htm
Xcell Journals	Quarterly journals for Xilinx programmable logic users http://support.xilinx.com/xcell/xcell.htm
Technical Tips	Latest news, design tips, and patch information for the Xilinx design environment http://support.xilinx.com/support/techsup/journals/index.htm

Conventions

This manual uses the following conventions. An example illustrates most conventions.

Typographical

The following conventions are used for all documents.

- `Courier font` indicates messages, prompts, and program files that the system displays.

```
speed grade: - 100
```

- **Courier bold** indicates literal commands that you enter in a syntactical statement. However, braces “{ }” in Courier bold are not literal and square brackets “[]” in Courier bold are literal only in the case of bus specifications, such as bus [7:0].

```
rpt_del_net=
```

Courier bold also indicates commands that you select from a menu.

File → **Open**

- *Italic font* denotes the following items.
 - ◆ Variables in a syntax statement for which you must supply values

```
edif2ngd design_name
```

- ◆ References to other manuals

See the *Development System Reference Guide* for more information.

- ◆ **Emphasis in text**

If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

- Square brackets “[]” indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

```
edif2ngd [option_name] design_name
```

- Braces “{ }” enclose a list of items from which you must choose one or more.

```
lowpwr = {on | off}
```

- A vertical bar “|” separates items in a list of choices.

```
lowpwr = {on | off}
```

- A vertical ellipsis indicates repetitive material that has been omitted.

```
IOB #1: Name = QOUT'
```

```
IOB #2: Name = CLKIN'
```

```
.  
. .  
. . .
```

- A horizontal ellipsis “...” indicates that an item can be repeated one or more times.

```
allow block block_name loc1 loc2 ... locn;
```

Online Document

The following conventions are used for online documents.

- **Blue text** indicates cross-references within a book. **Red text** indicates cross-references to other books. Click the colored text to jump to the specified cross-reference.
- **Blue, underlined text** indicates a Web site. Click the link to open the specified Web site. You must have a Web browser and internet connection to use this feature.

Contents

About This Manual

Manual Contents	v
Additional Resources	v

Conventions

Typographical	vii
Online Document	viii

Chapter 1 Introduction

Architecture Support	1-1
Overview	1-1
Features	1-2

Chapter 2 Getting Started

Install Package Definition	2-1
Setting Up your Environment	2-1
Proxy Settings	2-2
Web Browser Location	2-3
User Registration	2-3
Required Inputs for IP Update Packages	2-4
.....	2-5

Chapter 3 Install Cores Tool

Installing Cores using the Graphical User Interface	3-1
The Selection Pane	3-2
Selecting Packages to Install	3-2
Running Get Models	3-3

Introduction

This chapter provides an overview of the CORE Generator Update Installer tool and includes the following sections.

- “Architecture Support” section
- “Overview” section
- “Features” section

Architecture Support

The software supports the following architecture families in this release.

- Virtex™ /-II/-II PRO/-E
- Spartan™ /-II/-IIE/XL
- XC4000™ E/L/EX/XL/XLA

Overview

The Core Generator Update Installer is a CORE Generator utility which allows you to install CORE Generator IP and software updates from the Xilinx IP Center. The Update Installer tool extracts the files from the IP updates (.zip or .jar) and deposits them into your Xilinx installation directory.

In addition, the Update Installer can install user created cores packaged by the IP Capture tool. Refer to the IP Capture Tool User Guide for more information on packaging IP.

Features

The following is a list of features for the Core Generator Update Installer tool.

- Easy access from the CORE Generator "Tools" menu.
- Automatically displays the latest CORE Generator IP Updates available on the Xilinx Web site.
- Automatically loads the URL for each update package selected from the available packages list.
- Performs dependency checks and alerts you to packages that need to be installed first.
- Handles IP update package download(a URL must be specified), archive extraction, and log file creation.
- Automatically installs updates to the proper location.
- Detects IP and CORE Generator software updates which have already been installed.
- Automatically runs the Get Models utility to extract all HDL simulation models bundled with the downloaded IP package.
- Reports installation success or failure.

Getting Started

This chapter contains the following sections.

- [“Install Package Definition” section](#)
- [“Setting Up your Environment” section](#)

Install Package Definition

An Install Package is an archive or file in the .zip or .jar (JAVA Archive) format which contains files needed by the Update Installer to install an IP, or set of IP (the installer executables). The Install Package also contains files needed by the CORE Generator to support the generation of new cores and may also include updates to the CORE Generator software.

Setting Up your Environment

To take advantage of the Update Installer tool, you must ensure that your system can connect to the Internet. If you are operating behind a firewall, you need to configure your proxyHost and proxyPort settings.

Update Installer attempts to make an Internet connection every time you click on the *Add to Install Queue* or *Install All Cores From Queue* buttons. If the connection attempt times out, a pop-up dialog will appear, giving you the opportunity to change your proxy settings.

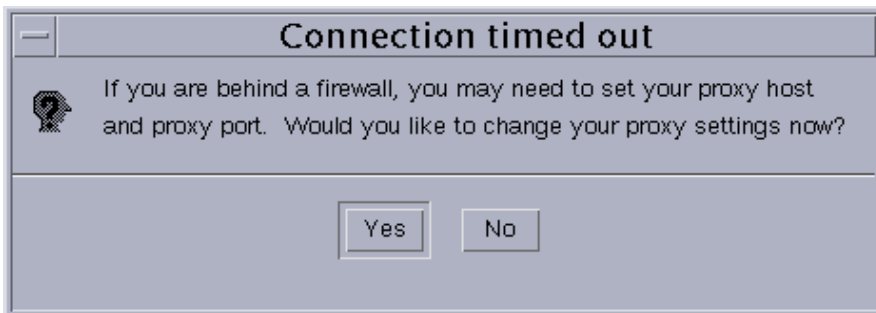


Figure 2-1 Connection Timed Out Dialog Box

The proxy settings can be set in the Proxy settings dialog box, as shown in the following figure.

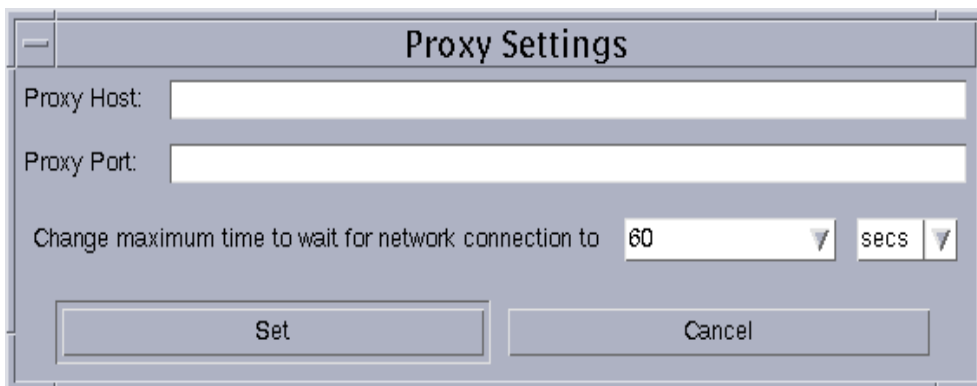


Figure 2-2 Proxy Settings Dialog Box

Proxy Settings

The Proxy Settings Dialog boxes contains the following fields.

1. Proxy Host: Contact your system administrator for the name of your ProxyHost
2. Proxy Port: By default, this field is set to Port 80.

Note Contact your system administrator if a different port setting is required.

3. **Max timeout:** This is the amount of time Update Installer will attempt to make a connection before asking whether you want to change your proxy settings or stop trying.

Note The default time your system waits before timing out may be shorter than the value specified here. You can not use this setting to make your system wait longer for a connection than it is allowed to.

If an Internet connection can not be made by the Update Installer Tool, you can still use the tool to install already downloaded packages. However, you will not be able to access information on what IP Updates packages are currently available or take advantage of the automated Web download process. You will need to download the IP Update archive(s) through your Web browser or via FTP and the IP update must be in the .zip or .jar file format (.tar files are not supported). Once the archives have been downloaded, you can install them using the Update Installer tool by specifying the explicit location of the downloaded archives.

Web Browser Location

Update Installer uses your Web browser to display any online documentation associated with an update package.

To specify the location of your web browser, follow these steps.

1. Select **CORE Generator's Projects** → **Preferences**
2. In the *Location of Web Browser* field, enter the appropriate path to your web browser.

User Registration

To download IP Update packages using the Update Installer tool, you must be registered with the Xilinx web site. To register, follow these steps.

1. Access the Xilinx website, <http://www.xilinx.com> through your web browser.
2. Click on the *my profile* link at the lower lefthand corner of this web page.
3. Click on the *new customers please register* link and complete the registration questions

Once you are registered, you can access IP updates through the Update Installer's User Login dialog box.

You may also need to be registered at the IP Update lounge to access a given IP package. For example, to access the standard CORE Generator Updates, access the registration link on

<http://www.xilinx.com/ipcenter/coregen/updates.htm>



Figure 2-3 User Login Dialog Box

Required Inputs for IP Update Packages

The Install Cores tool requires information on the location of each IP update package it must install. The following list explains how the location information can be specified.

1. A URL pointing to the zip/jar archive corresponding to the update
2. A fully qualified or relative path to the zip/jar file on your local hard drive

Note Use this option if you already downloaded an IP Update to your local hard drive, but would like to have Update Installer install the downloaded package.

CORE Generator Update Installer Tool

This chapter contains the following sections.

- “Installing Cores using the Graphical User Interface” section
- “Running Get Models” section

Installing Cores using the Graphical User Interface

The Update Installer Tool Graphical User Interface allows centralized access to packages available for installation and to packages already installed.

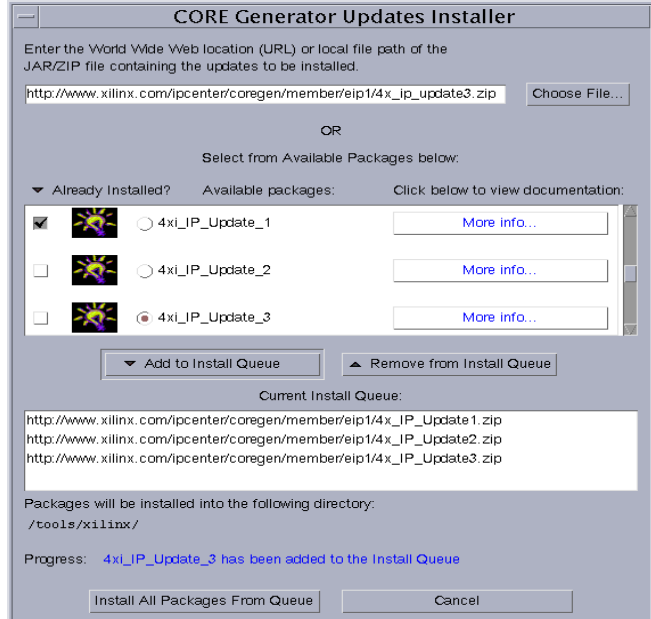


Figure 3-1 Install Cores

The Selection Pane

The scrollable center region of this GUI displays a list of packages that are available for installation. Each Row corresponds to a single install package and is divided into three fields, as described below.

- **Already Installed** - The *already Installed* field consists of a non-editable status checkbox which indicates whether the corresponding package is already installed
- **Available Packages** - The *available packages* field allows you to select which package you want to add to the Install Queue.
- **View Documentation** - The *click below to view documentation field* provides a link to online documentation for the package.

If your proxy settings are not configured correctly, or if you are unable to connect to the Xilinx IP Center, the *package selection pane* will not display in the GUI. If this occurs, you must manually enter the URL or the explicit path to the packages you wish to install.

Selecting Packages to Install

To install packages in an Install Cores session, follow these steps.

1. To add a package to the Install Queue, use the *Choose File Button* to browse to the location of the package you wish to install.

Note You can also select packages from the center selection pane region to automatically load the file location into the text field

2. Click the Add to Install Queue button to add your selection to the Install Queue.

Note The Progress field at the bottom of the GUI will inform you of the status of this process

3. If you want to add another package to the install queue, repeat steps 1 and 2.
4. To install all the packages in the current install queue, select the *Install All Cores from Queue* button.

Note The CORE Generator application will close and a confirmation dialog box will display when the install is complete. The exact amount of time of this process will depend on the size and number of packages you are installing.

Running Get Models

As part of the installation process, the Install Cores Tool automatically runs the Get Models tool after the extraction process is complete for each IP package. (Certain packages contain specific instructions indicating that Get Models should not be run.) The confirmation dialog that appears at the end of the extraction process will indicate when Get Models is invoked. The Get Models is run once for each package that is installed.

Get Models extracts the HDL behavioral models of the cores it has installed and copies them to `$XILINX/verilog/src/XilinxCoreLib` and `$XILINX/vhdl/src/XilinxCoreLib`, respectively. It also updates analyze order files (`$XILINX/verilog/src/XilinxCorelib/verilog_analyze_order` and `$XILINX/vhdl/src/XilinxCoreLib/vhdl_analyze_order`) which specify the order in which the simulation models should be compiled for pre-compiled HDL simulators.