PCI-X Interface v5.0

DS208 August 31, 2005 Product Specification v5.0.101

Features

- Fully PCI-X 2.0 Mode 1 compliant LogiCORE™, 64-bit, 133/66 MHz interface with 3.3 V operation
- PCI 3.0-compliant core up to 33 MHz
- Customizable, programmable, single-chip solution
- Pre-defined implementation for predictable timing
- Incorporates Xilinx Smart-IP™ Technology
- Fully verified design tested with Xilinx proprietary testbench and hardware
- Available through the Xilinx CORE Generator™ system v7.1i or higher
- Integrated extended capabilities:
  - PCI-X Capability Item
  - Power Management Capability Item
  - Message Signalled Interrupt Capability Item
- Supported PCI-X only functions
  - Split Completion
  - Memory Read DWORD
  - Memory Read Block
  - Memory Write Block
- Supported PCI only functions
  - Memory Read
  - Memory Read Multiple
  - Memory Read Line
  - Memory Write and Invalidate

LogiCORE Facts	
PCI-X64/66 with PCI64/33 Resource Utilization(1)	
LUTs	2812
Slice Flip Flops	1622
IOB Flip Flops	257
IOBs	90
BUFGs / DCMs	2/1
PCI-X64/66 Mode Only Resource Utilization (1)	
LUTs	2186
Slice Flip Flops	1484
IOB Flip Flops	257
IOBs	90
BUFGs / DCMs	1/1
PCI64/33 Mode Only Resource Utilization (1)	
LUTs	1868
Slice Flip Flops	1350
IOB Flip Flops	253
IOBs	90
BUFGs / DCMs	1/0(4)
PCI-X64/133 and PCI-X 64/100 Resource Implementation (1)	
Slice Four Input LUTs	2310
Slice Flip Flops	1504
IOBs	90
BUFGs/DCMs	1/1
Provided with Core	
Documentation	*PCI-X Product Specification* *PCI-X Getting Started Guide* *PCI-X User Guide*
Design File Formats	Verilog/VHDL Simulation Model NGO Netlist
Constraints Files	User Constraints Files (UCF)
Example Design	Verilog/VHDL Example Design
Design Tool Requirements	
Xilinx Tools	v7.1i Service Pack 4
Tested Entry and Verification Tools (2)	Synplicity Synplify Xilinx XST (3) Model Technology ModelSim Exemplar LeonardoSpectrum Cadence NC-Verilog
Xilinx provides technical support for this product when used as described in the *Getting Started Guide* and the *User Guide*. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices not listed, or if customized beyond that allowed in the product documentation.	

Fact Table Notes

1. Resource utilization depends on configuration of the interface and the user design. Unused resources are trimmed by the Xilinx technology mapper. The utilization figures reported in this table are representative of a maximum configuration.
2. See the *PCI-X Getting Started Guide* or product release notes for current supported versions.
3. XST is command line option only. See the *PCI-X Getting Started Guide* for details.
4. Virtex-4 implementations require additional BUFG for 200MHz reference clock.

Table 1: **Core Implementation for PCI-X64**

Device Supported	Power Supply
PCI64/33	
Virtex™-E XCV300E-BG432-8C	3.3V only
Virtex-II XC2V1000-FG456-5C/I	3.3V only
Virtex-II Pro XC2VP7-FF672-6C/I	3.3V only
Virtex-II Pro XC2VP20-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP30-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP40-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP50-FF1152-6C/I	3.3V only
Virtex-4 XC4VLX25-FF668-10C/I (6,7)	3.3V only
Virtex-4 XC4VSX35-FF668-10C/I (6,7)	3.3V only
Virtex-4 XC4VFX20-FF672 -10C/I (6,7)	3.3V only
PCI-X64/66	
Virtex-E XCV300E-BG432-8C	3.3V only
Virtex-II XC2V1000-FG456-5C/I	3.3V only
Virtex-II Pro XC2VP7-FF672-6C/I	3.3V only
Virtex-II Pro XC2VP20-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP30-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP40-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP50-FF1152-6C/I	3.3V only
Virtex-4 XC4VLX25-FF668-10C/I (6)	3.3V only
Virtex-4 XC4VSX35-FF668-10C/I (6)	3.3V only
Virtex-4 XC4VFX20-FF672-10C/I (6)	3.3V only
PCI-X64/100	
Virtex-II XC2V1000-FG456-5C/I	3.3V only
Virtex-II Pro XC2VP7-FF672-6C/I	3.3V only
Virtex-II Pro XC2VP20-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP30-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP40-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP50-FF1152-6C/I	3.3V only
Virtex-4 XC4VLX25-FF668-10C/I (6)	3.3V only
Virtex-4 XC4VSX25-FF668-10C/I (6)	3.3V only

Table 1: **Core Implementation for PCI-X64 *(Continued)***

Device Supported	Power Supply
Virtex-4 XC4VFX25-FF668-10C/I (6)	3.3V only
PCI-X64/133	
Virtex-II XC2V1000-FG456-6C/I	3.3V only
Virtex-II Pro XC2VP7-FF672-6C/I	3.3V only
Virtex-II Pro XC2VP20-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP30-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP40-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP50-FF1152-6C/I	3.3V only
Virtex-4 XC4VLX25-FF668-10C/I (6)	3.3V only
Virtex-4 XC4VSX25-FF668-10C/I (6)	3.3V only
Virtex-4 XC4VFX25-FF668-10C/I (6)	3.3V only
PCI-X64/66, PCI64/33 with Dual-Mode Bitstream	
Virtex-II XC2V1000-FG456-5C/I	3.3V only
Virtex-II Pro XC2VP7-FF672-6C/I	3.3V only
Virtex-II Pro XC2VP20-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP30-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP40-FF1152-6C/I	3.3V only
Virtex-II Pro XC2VP50-FF1152-6C/I	3.3V only

Notes

1. Fully compliant designs over 66 MHz require two bitstreams.
2. Universal card implementations not supported.
3. Commercial devices only; 0 C < T_j < 85 C.
4. Virtex-II Pro and Virtex-4 devices are supported over commercial and industrial temperature ranges.
5. Virtex-II 2v1000 is supported over commercial and industrial temperature ranges.
6. As shipped, the core is verified for timing compliance with speedfile versions 1.56 and later. This applies to all production devices and most engineering samples. If you are using engineering samples that require the 1.54 speedfile, please contact Xilinx Customer Applications.
7. Requires 200 MHz reference clock.

Additional Features

- Supported PCI and PCI-X functions
  - Memory Write
  - I/O Read
  - I/O Write
  - Configuration Read
  - Configuration Write
  - Interrupt Acknowledge
  - Bus Parking
  - Type 0 Configuration Space Header
  - Full 64-bit Addressing Support
  - Up to 6 Base Address Registers

- Expansion ROM Base Address Register
- Instant-On Base Address Registers
- Parity Generation, Parity Error Detection
- Full Command/Status Registers

Applications

- Embedded applications in networking, industrial, and telecommunication systems
- PCI-X add-in boards such as frame buffers, network adapters, and data acquisition boards
- Hot swap CompactPCI-X boards
- Any applications that need a PCI-X interface

General Description

The PCI-X Interface is a pre-implemented and fully tested module for Xilinx FPGAs. Critical paths are controlled by constraints files to ensure predictable timing. This significantly reduces engineering time required to implement the PCI-X portion of your design. Resources can instead be focused on your unique user application logic in the FPGA and on the system-level design. As a result, Xilinx PCI-X products minimize your product development time.

The core meets the setup, hold, and clock-to-timing requirements as specified in the PCI-X specification. The interface is verified through extensive simulation.

Other features that enable efficient implementation of a PCI-X system include:

- **Block SelectRAM™ memory**: Blocks of on-chip ultra-fast RAM with synchronous write and dual-port RAM capabilities. Used in PCI-X designs to implement FIFOs.
- **SelectRAM memory**: Distributed on-chip ultra-fast RAM with synchronous write option and dual-port RAM capabilities. Used in PCI-X designs to implement FIFOs.

The PCI-X interface is carefully optimized for best possible performance and utilization in Xilinx FPGA devices.

Smart-IP Technology

Drawing on the architectural advantages of Xilinx FPGAs, Xilinx Smart-IP technology ensures the highest performance, predictability, reproducibility, and flexibility in PCI-X designs. The Smart-IP technology is incorporated in every PCI-X Interface.

Xilinx Smart-IP technology leverages the Xilinx architectural advantages, such as look-up tables and segmented routing, as well as floorplanning information, such as logic mapping and location constraints. This technology provides the best physical layout, predictability, and performance. Additionally, these features allow for significantly reduced compile times over competing architectures.

To guarantee the critical setup, hold, minimum clock-to-out, and maximum clock-to-out timing, the PCI-X interface is delivered with Smart-IP constraints files that are unique for a device and package combination. These constraints files guide the implementation tools so that the critical paths are always within specification.

Xilinx provides Smart-IP constraints files for many device and package combinations. Constraints files for unsupported device and package combinations may be generated using the web-based user constraints file generator.

Functional Description

Figure 1 illustrates the PCI-X Interface partitioned into six major blocks and a user application.

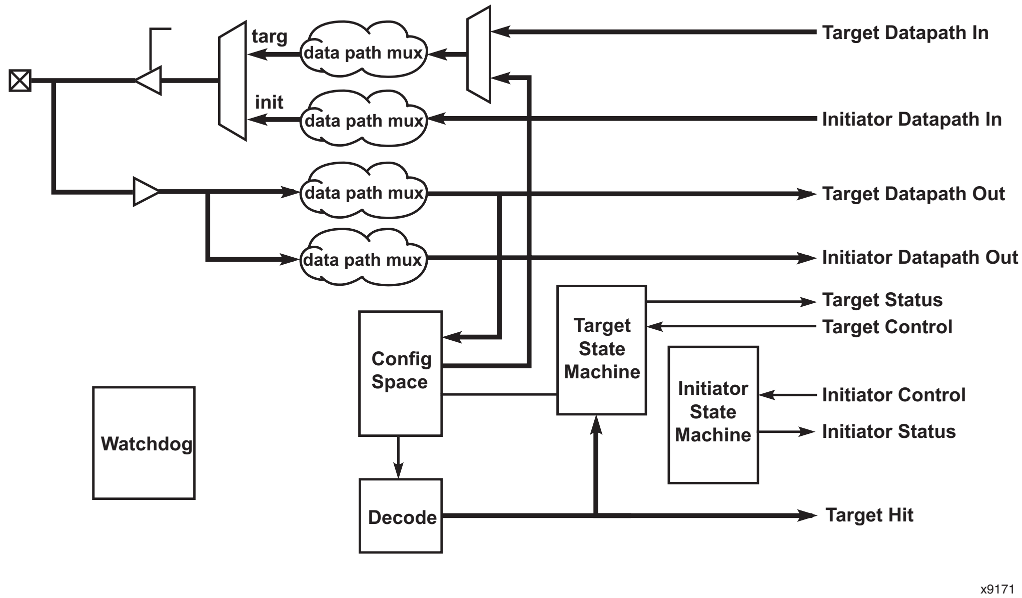

Figure 1: **PCI-X Interface Block Diagram**

Datapath

There are four datapaths, in and out for both target and initiator. To improve timing and ease of design, the four unidirectional datapaths are multiplexed inside the interface. All data transfers are register-to-register. Since fewer registers are on each datapath, loading is reduced and false timing paths are eliminated.

Decode

When an address is broadcast on the bus, the decode module compares it to the base address registers for a match. If one occurs, the target state machine is activated.

PCI-X Configuration Space

This block provides the first 64 bytes of Type 0, version 3.0 Configuration Space Header, and an additional 64 bytes reserved for extended capabilities, as shown in Table 2. The remaining 128 bytes of configuration space is available to the user for application specific registers. Together, these support software-driven Plug-and-Play initialization and configuration. This includes information for Command, Status, Base Address Registers, and the extended capabilities required for PCI-X. Three extended capabilities are provided in the interface:

- PCI-X Capability Item
- Power Management Capability Item
- Message Signalled Interrupt Capability Item

These capability items may be linked or delinked from the capabilities list as required, and user functions can be integrated into the capabilities list.

Table 2: **PCI-X Configuration Space Header**

31	16	15	0	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Rev ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
Base Address Register 0 (BAR0)				10h
Base Address Register 1 (BAR1)				14h
Base Address Register 2 (BAR2)				18h
Base Address Register 3 (BAR3)				1Ch
Base Address Register 4 (BAR4)				20h
Base Address Register 5 (BAR5)				24h
Cardbus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			CapPtr	34h
Reserved				38h
Max Lat	Min Gnt	Interrupt Pin	Interrupt Line	3Ch
Power Management Capability		NxtCap	PM Cap	40h
Data	PMCSR BSE	PMCSR		44h
Message Control		NxtCap	MSI Cap	48h
Message Address				4Ch
Message Upper Address				50h
Reserved		Message Data		54h
PCI-X Command		NxtCap	PCI-X Cap	58h
PCI-X Status				5Ch
Reserved				60h-7Fh
Available User Configuration Space				80h-FFh

Note: Shaded areas are not implemented and return zero.

Watchdog

The watchdog monitors various system conditions, including bus mode and bus width. This module also indicates if run-time reconfiguration is required for loading different bitstreams.

Target State Machine

This block controls the PCI-X and PCI interface for target functions. The controller is a high-performance state machine using one-hot encoding for maximum performance.

Initiator State Machine

This block controls the PCI-X and PCI interface for initiator functions. The initiator control logic also uses one-hot encoding for maximum performance.

User Interface

The PCI-X interface provides a simplified user application interface which allows a user to create one design that handles both PCI-X and PCI transactions without design changes, and both 32-bit and 64-bit data transfers without external data width conversion. This eliminates the need for multiple designs to support PCI-X and PCI and varying bus widths.

This streamlined interface also simplifies the amount of work needed to create a user application. The user interface can be designed as either a 32-bit or 64-bit interface and the PCI-X interface will automatically handle data conversions regardless of the width of the PCI-X or PCI bus.

Interface Configuration

The PCI-X Interface can be easily configured to fit unique system requirements using the Xilinx CORE Generator GUI or by changing the HDL configuration file. The following customization options, among many others, are supported by the interface and are described in the *PCI-X User Guide.*

- Device and vendor ID
- Base Address Registers (number, size, and mode)
- Expansion ROM BAR
- Cardbus CIS pointer
- Interrupt Connectivity
- Extended Command Use
- Capability Configuration

Burst Transfer

The PCI-X bus derives its performance from its ability to support burst transfers. The performance of any PCI-X application depends largely on the size of the burst transfer. Buffers to support PCI-X burst transfer can efficiently be implemented using on-chip RAM resources.

Supported PCI Commands

Table 3 defines the PCI bus commands supported by the PCI-X Interface, and Table 4 defines the supported PCI-X bus commands.

Table 3: **PCI Bus Commands**

CBE [3:0]	Command	Initiator	Target
0000	Interrupt Acknowledge	Yes	Yes
0001	Special Cycle	Yes	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read[1]	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	Ignore	Ignore
1001	Reserved	Ignore	Ignore
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Memory Read Multiple[2]	Yes	Yes
1101	Dual Address Cycle	Yes	Yes
1110	Memory Read Line[2]	Yes	Yes
1111	Memory Write Invalidate[2]	Yes	Yes

Notes

1. This command can only be used for a single DWORD transfer.
2. These commands have fixed byte enables of `0h`.

Table 4: **PCI-X Bus Commands**

CBE [3:0]	Command	Initiator	Target
0000	Interrupt Acknowledge	Yes	Yes
0001	Special Cycle	Yes	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read Dword	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Alias to Memory Read Block	Yes	Yes
1001	Alias to Memory Write Block	Yes	Yes
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Split Completion	Yes	Yes
1101	Dual Address Cycle	Yes	Yes
1110	Memory Read Block	Yes	Yes
1111	Memory Write Block	Yes	Yes

Bandwidth

The PCI-X Interface supports fully compliant zero wait-state burst operations for both sourcing and receiving data. This interface supports a sustained bandwidth of up to 1066MBytes/sec. The design can be configured to take advantage of the ability of the PCI-X Interface to do very long bursts.

The flexible user application interface, combined with support for many different PCI-X features, gives users a solution that lends itself to use in many high-performance applications. The user is not locked into one DMA engine, hence, an optimized design that fits a specific application can be designed.

Recommended Design Experience

The PCI-X Interface is pre-implemented allowing engineering focus on the unique user application functions of a PCI-X design. Hwoever, PCI-X is a high-performance design that is challenging to implement in any technology. For this reason, previous experience building high-performance, pipelined FPGA designs using Xilinx implementation software, constraint files, and guide files is recommended. The challenge to implement a complete PCI-X design including user application functions varies depending on configuration and functionality of your application. Contact your local Xilinx representative for a closer review and estimation for your specific requirements.

Timing Specifications

The maximum speed at which your user design is capable of running can be affected by the size and quality of the design. The key timing parameters for the PCI-X 133 MHz are shown in Table 6; for the PCI-X 66MHz in Table 5, and for the PCI 33MHz in Table 7.

Table 5: **Timing Parameters for PCI-X 66 MHz**

Symbol	Parameter	Min	Max
T_{cyc}	CLK Cycle Time	15[1]	20
T_{high}	CLK High Time	6	-
T_{low}	CLK Low Time	6	-
T_{val}	CLK to Signal Valid Delay (bused signals)	0.7[2]	3.8[2]
T_{val}	CLK to Signal Valid Delay (point to point signals)	0.7[2]	3.8[2]
T_{on}	Float to Active Delay	0[2]	-
T_{off}	Active to Float Delay	-	7[2]
T_{su}	Input Setup Time to CLK (bused signals)	1.7[2]	-
T_{su}	Input Setup Time to CLK (point to point signals)	1.7[2]	-
T_h	Input Hold Time from CLK	0.5[2]	-
T_{rstoff}	Reset Active to Output Float	-	40

Notes

1. Controlled by timespec constraints, included in product.
2. Controlled by SelectIO configured for PCIX.
3. Operation at 100 MHz requires T_{su} of 1.2 and T_{cyc} of 10.

Table 6: **Timing Parameters for PCI-X 133 MHz**

Symbol	Parameter	Min	Max
T_{cyc}	CLK Cycle Time	7.5[1]	20
T_{high}	CLK High Time	6	-
T_{low}	CLK Low Time	6	-
T_{val}	CLK to Signal Valid Delay (bused signals)	0.7[2]	3.8[2]
T_{val}	CLK to Signal Valid Delay (point to point signals)	0.7[2]	3.8[2]
T_{on}	Float to Active Delay	0[2]	-
T_{off}	Active to Float Delay	-	7[2]
T_{su}	Input Setup Time to CLK (bused signals)	1.2[2]	-
T_{su}	Input Setup Time to CLK (point to point signals)	1.2[2]	-
T_h	Input Hold Time from CLK	0.5[2]	-
T_{rstoff}	Reset Active to Output Float	-	40

Notes
1. Controlled by timespec constraints, included in product.
2. Controlled by SelectIO configured for PCIX.
3. Operation at 100 MHz requires T_{su} of 1.2 and T_{cyc} of 10.

Table 7: **Timing Parameters for PCI 33 MHz**

Symbol	Parameter	Min	Max
T_{cyc}	CLK Cycle Time	30[1]	-
T_{high}	CLK High Time	11	-
T_{low}	CLK Low Time	11	-
T_{val}	CLK to Signal Valid Delay (bused signals)	2[2]	11[2]
T_{val}	CLK to Signal Valid Delay (point to point signals)	2[2]	11[2]
T_{on}	Float to Active Delay	2[2]	-
T_{off}	Active to Float Delay	-	28[1]
T_{su}	Input Setup Time to CLK (bused signals)	7[2]	-
T_{su}	Input Setup Time to CLK (point to point signals)	10[2]	-
T_h	Input Hold Time from CLK	0[2]	-
T_{rstoff}	Reset Active to Output Float	-	40

Notes
1. Controlled by timespec constraints, included in product.
2. Controlled by SelectIO configured for PCI33_3 or PCIX.

Ordering Information

Build v5.0.100 of the PCI-X core is available for download from the Xilinx **IP Center** and can also be accessed through the Xilinx CORE Generator system v7.1i or higher. The Xilinx CORE Generator software is bundled with the ISE Foundation v7.1i software at no additional charge. To purchase the Xilinx PCI-X core, please contact your local Xilinx **sales representative**.

Part Numbers

- DO-DI-PCIX64-VE
  - PCI-X 64-bit 66/133 MHz IP only core
- DX-DI-64IP-XVE
  - Upgrade from DO-DI-PCI64/DO-DI-PCI-AL/DO-DI-PCI64DK to DO-DI-PCIX64-VE

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/28/02	1.0	New template
11/04/02	1.1	Update for core compliance of 2.0 Mode1; performance of 64-bit/133 MHz; support of PCI v2.3; support of Xilinx design tool v5.li Service Pack 2.
12/05/02	1.2	In Introduction section, 1066 Mbytes/sec was 800 Mbytes/sec; in Features section, first bullet, 133/66 MHz was 133/66/33 MHz
3/03/03	1.3	Revised date to 3/7/03; added PCI-X64/PCI-X64/100 Resource Utilization data; revised Xilinx tools to v5.2i; added Virtex-II Pro to PCI-X 64 Supported Devices list.
4/17/03	1.4	Revised date to 4/14/03; in Table 4, Clock Cycle Time, Min 7.5 was Min 15; Input Setup Time to CLK (bused signals) and Input Setup Time to CLK (point to point signals), Min 1.2 was Min 1.7.
5/8/03	1.5	Updated Xilinx tools to 5.2i SP2.
5/29/03	1.6	In LogiCORE table, speed grade for PCI-X 64/133 only, Virtex-II 2VP7FF672 device changed to -7C; was 6C
9/17/03	1.7	In LogiCORE Facts table, Xilinx Tools v6.1i SP1 was v5.2i SP2; date was May 29, 2003.
11/14/03	1.8	In Supported Devices table, added XC prefix to all device numbers; changed all PCI-X 64/133 devices to XC2VP7FF672-6 was -7; Xilinx Tools v6.1i SP2 was v6.1i SP1;
1/25/04	1.9	In LogiCORE table, changed Xilinx Tools to v6.1i SP3; in Supported Devices table, added Virtex-Pro XC2VP20FF1152-6C in each family group; in first page, changed year date to 2004.
3/10/04	1.10	Updated to v3.0.126, updated Xilinx tools to 6.2i SP1, added note 11 to Supported devices table, added suffix /I to all Virtex-II Pro devices, added Virtex-II Pro XC2VP30...through XC2VP50...to each supported category.
4/26/04	1.11	Updated build version to v5.0.78, updated Xilinx tools to 6.2i SP2, changed date to April 26, 2004.
7/15/04	1.12	Updated build to v5.0.79, and added support for Xilinx tools v6.2i SP3. The data sheet is updated to the new template.

Date	Version	Revision
9/23/04	1.13	Updated document to fix a typographical error in the Core Implementation table on page 3.
11/11/04	1.14	Updated support for Xilinx tools v6.3i; updated PCI spec to v3.0; added Exemplar LeonardoSpectrum and Cadence NC-Verilog entry and verification tools.
12/8/04	1.15	Updated to build 5.0.90 and Virtex-4 support.
3/7/05	1.16	Updated to Xilinx tools 7.1i and PCI-X build 5.0.95.
5/13/05	2.0	Updated build to 3.0.150, added support for Spartan-3E, addition of SP2.
8/31/05	3.0	Updated build to 3.0.151, updated SP2 to SP4 for 7.1i