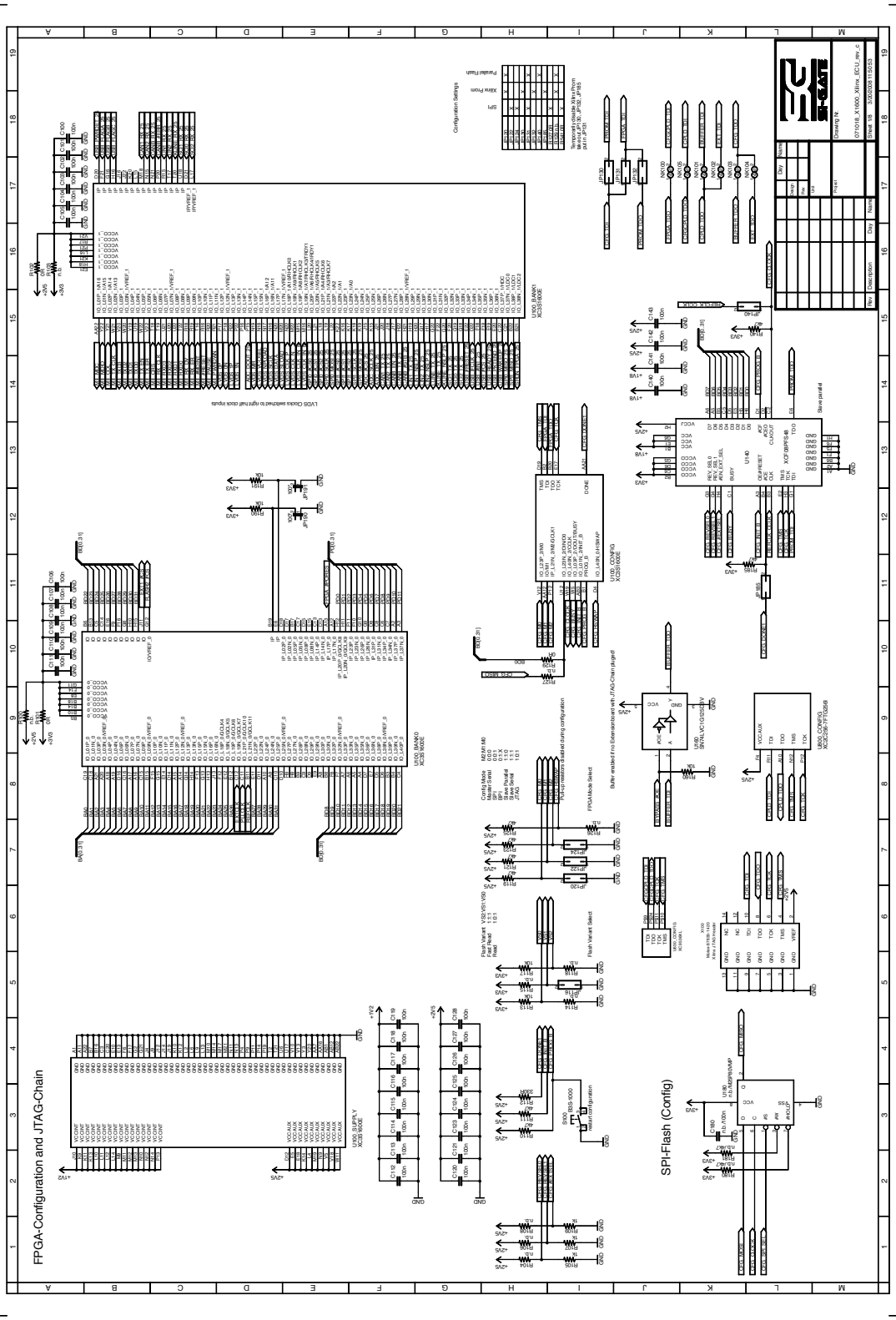
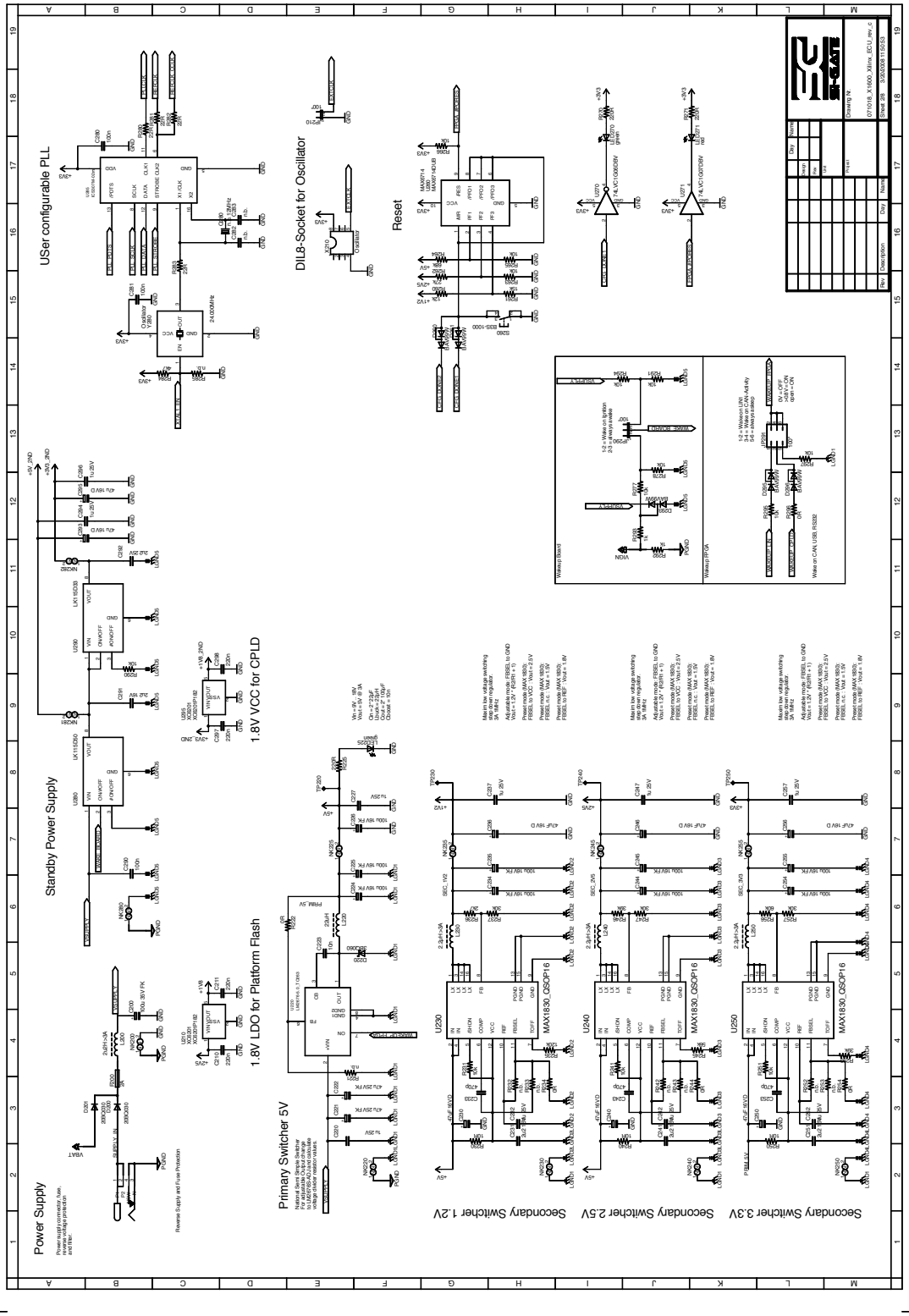

FPGA-Configuration and JTAG-Chain
SPI-Flash (Config)
U100_BANK0
XC3S1600E
U101_BANK1
XC3S1600E
U102_BANK2
XC3S1600E
U103_BANK3
XC3S1600E
U105_SUPPLY
XC3S1600E
U110_CONFIG
XC3S1600E
U800_CONFIG
XC2C256-TPG208
U140
XCF08PFS48
U180
M25P05-VMN6P
Slave parallel
Configuration Settings
Temporarily disable Xilinx Prom
Write Protect, PROG_B pull to JP30
Buffer enabled if no Extension(s) are left in JTAG-Chain (in use)
Pull up resistors tested during configuration
FPGA Mode Select
Flash Variant Select
Master configuration
LVDS Clocks switched to right half clock inputs
Reset Button
Reset Button
Reset Button


USer configurable PLL
DIL8-Socket for Oscillator
Reset
Standby Power Supply
1.8V VCC for CPLD
1.8V LDO for Platform Flash
Primary Switcher 5V
Power Supply
Secondary Switcher 1.2V
Secondary Switcher 2.5V
Secondary Switcher 3.3V
Wakeup Board
Wakeup RF-IA
Wake on CAN USB RS232
SI-CAT
Drawing No.
071018_X1600_Xilinx_ECU_rev_c
Sheet 2/8
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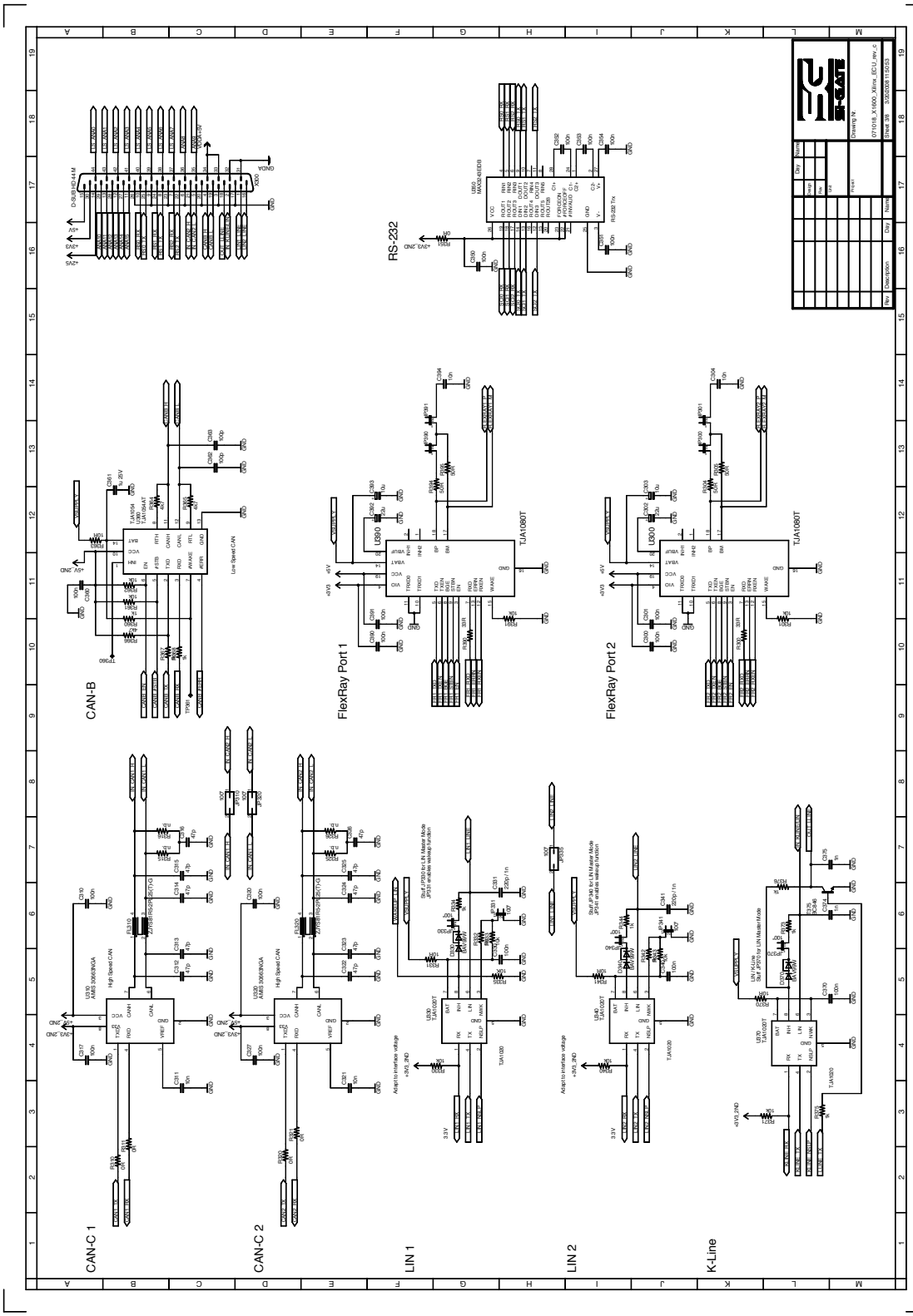
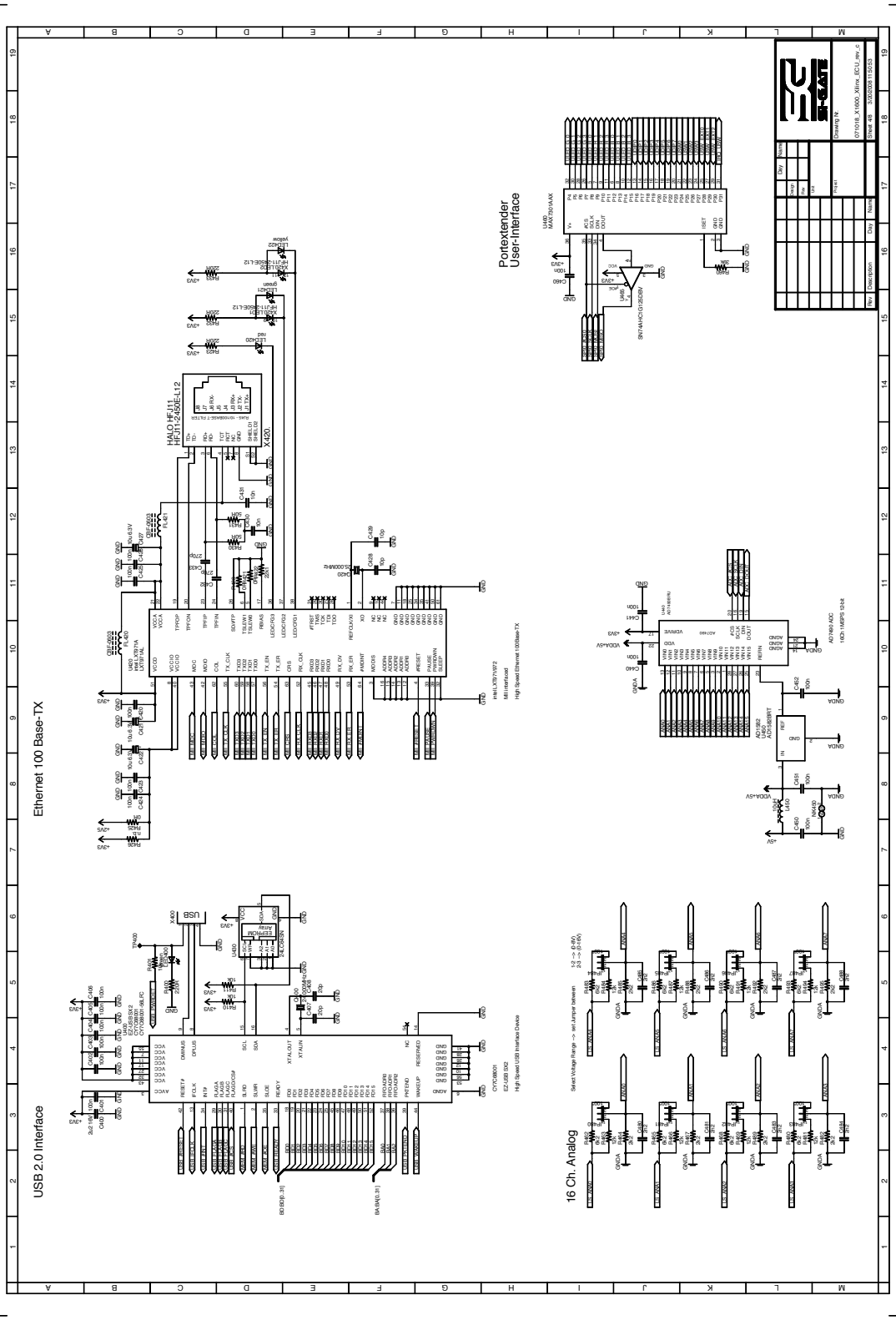

RS-232
CAN-B
FlexRay Port 1
FlexRay Port 2
CAN-C 1
CAN-C 2
LIN 1
LIN 2
K-Line


Ethernet 100 Base-TX
USB 2.0 Interface
16 Ch. Analog
Portextender
User-Interface
HALO HFJ11
HFJ11-2450E-L12
X420
USB
Intel LXT971QF2
Mii Interface
High Speed Ethernet 100Base-TX
CY7C68001
EZ-USB SX2
High Speed USB Interface Device
AD7490 ADC
16Ch 1MSPS 12bit
MAX3014AX
SN74HC10125DR
Select Voltage Range -> set Jumper between:
1-2 -> (0-5V)
2-3 -> (0-10V)
Drawing No.
071018_X1600_Xilinx_ECU_rev_c
Sheet 4/8
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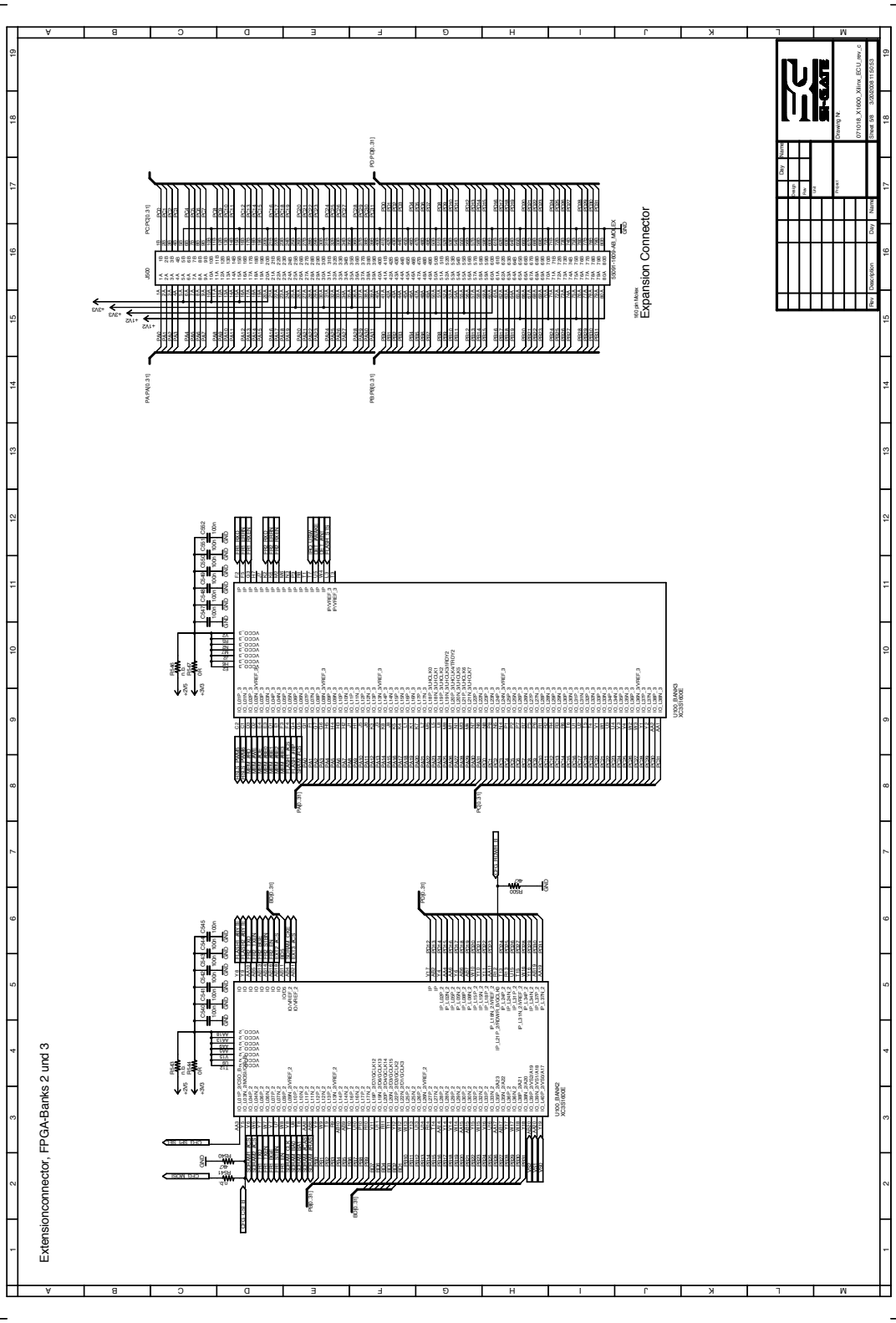
Extensionconnector, FPGA-Banks 2 und 3
Expansion Connector
U1D0 BANK0
XC3S1600E
U1D0 BANK2
XC3S1600E
Si-GATE
071018_X1600_Xilinx_ECU_rev_c
Sheet 5/8
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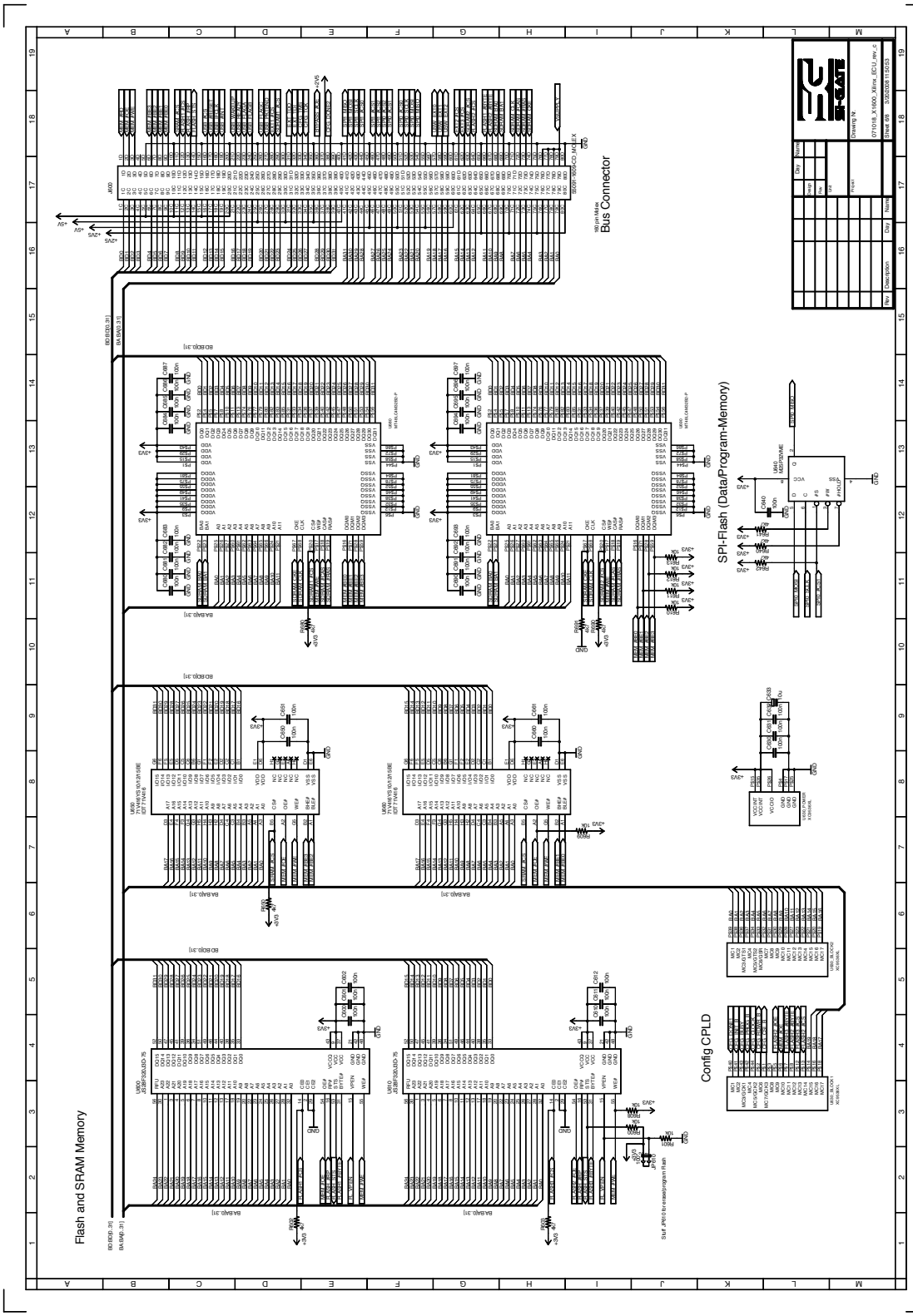
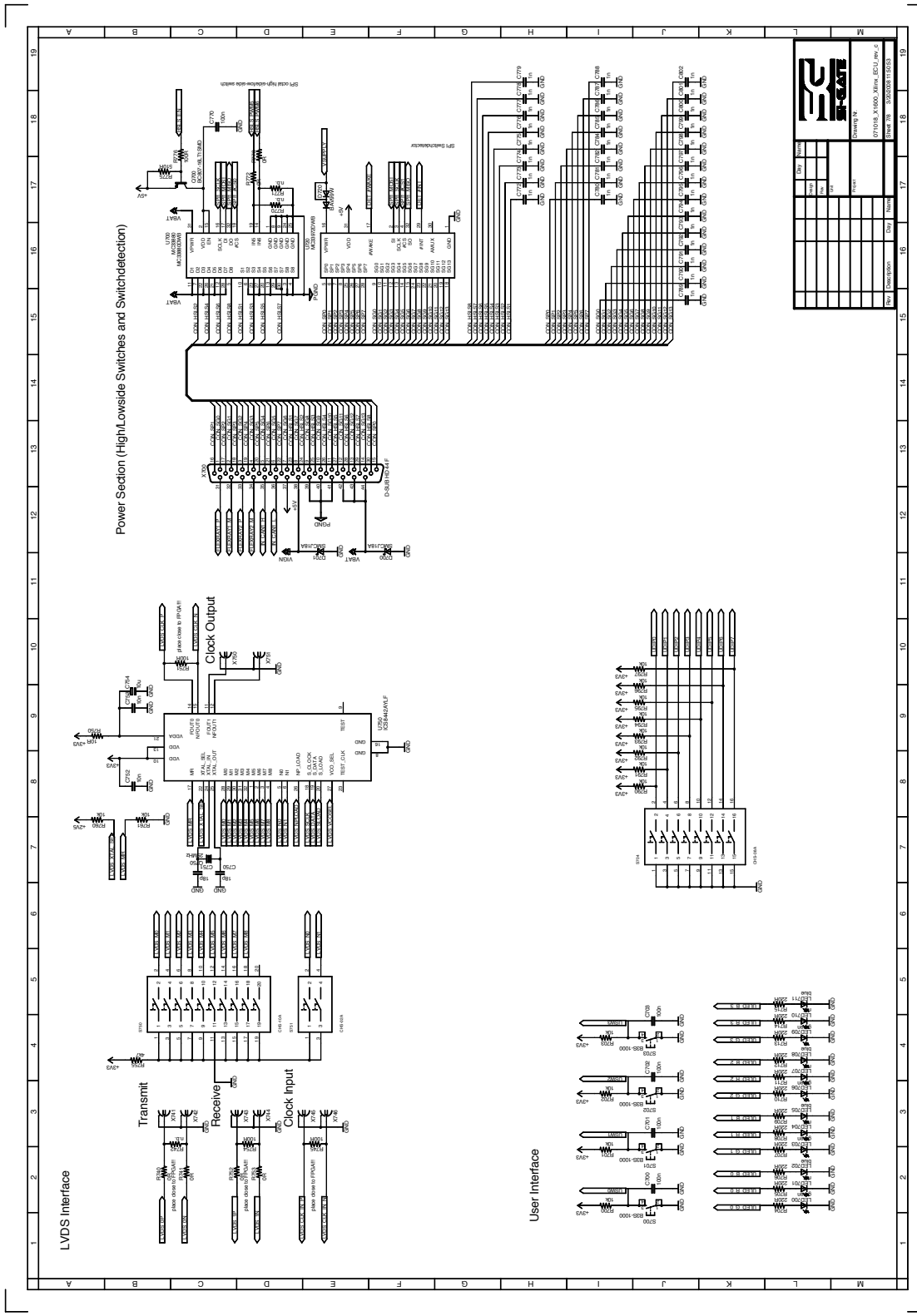

Flash and SRAM Memory
Bus Connector
SPI-Flash (Data/Program-Memory)
Config CPLD
071018_X1600_Xilinx_ECU_rev_c
Sheet 6/8
3/20/2008 11:55:53


Power Section (High/Lowside Switches and Switchdetection)
Clock Output
LVDS Interface
Transmit
Receive
Clock Input
User Interface
SI-EAT
071018_X1600_Xilinx_ECU_rev_c
Sheet 7/8
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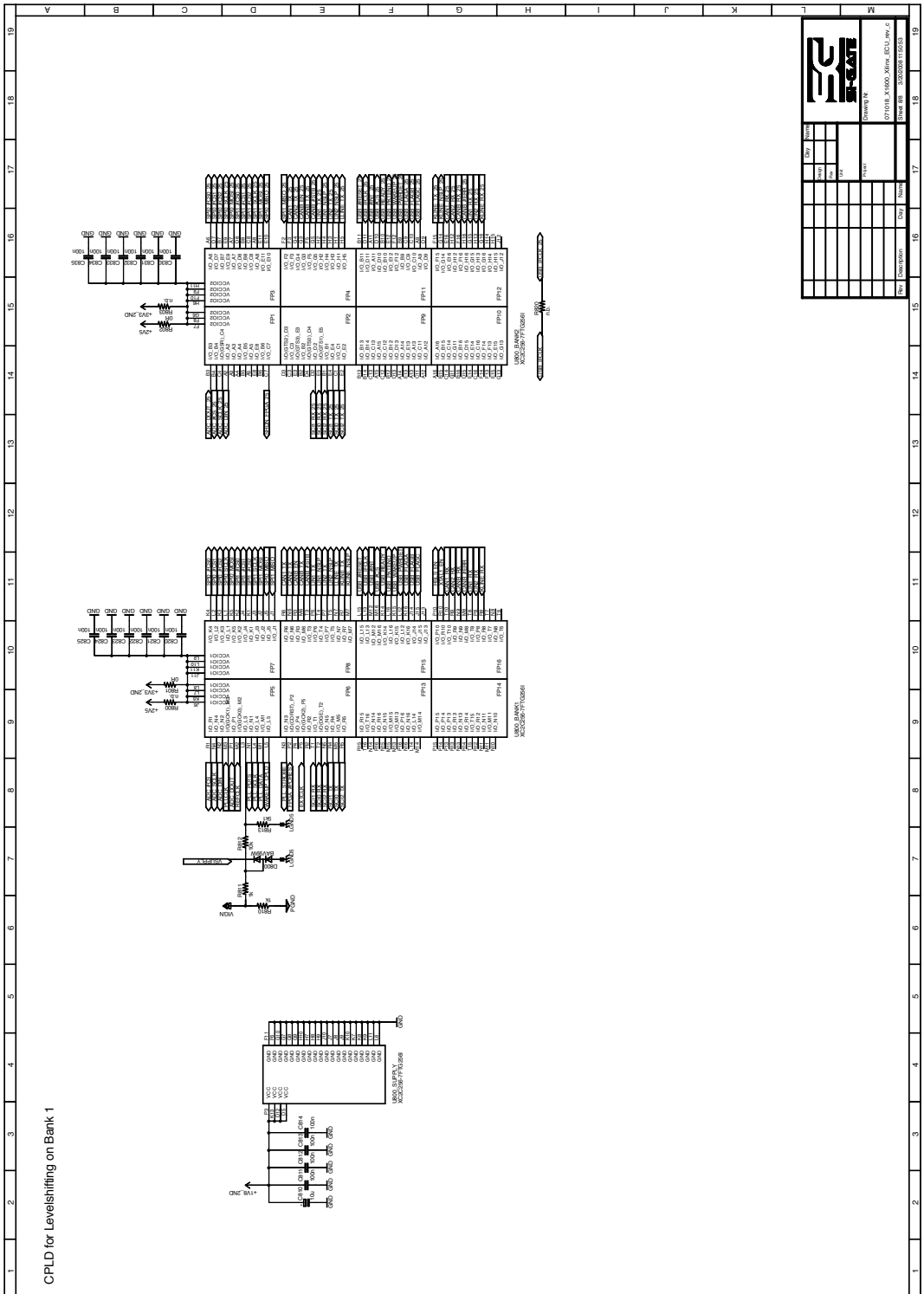
CPLD for Levelshifting on Bank 1
Drawing No
071018_X1600_Xilinx_ECU_rev_c
Sheet 8/8
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