

Getting Started with the ML300

Virtex-II Pro Development System

GVDT111 (v1.2) January 29, 2003





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The following table shows the revision history for this document..

	Version	Revision
12/23/02	1.0	Initial Xilinx release.
01/28/03	1.1	Converted document to book format.
01/29/03	1.2	Minor edits to text.

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About This Manual

Manual Contents

This manual contains the following chapter:

- “Getting Started with the ML300,” which provides an overview of the contents of the ML300 Evaluation Platform, directions on how to start using your ML300, and references to more information.

Additional Resources

For additional information, go to <http://support.xilinx.com>. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records http://support.xilinx.com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm
Data Book	Pages from <i>The Programmable Logic Data Book</i> , which contains device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging http://support.xilinx.com/partinfo/databook.htm
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues http://support.xilinx.com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment http://www.support.xilinx.com/xlnx/xil_tt_home.jsp

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Courier font	Messages, prompts, and program files that the system displays	speed grade: - 100
Courier bold	Literal commands that you enter in a syntactical statement	ngdbuild <i>design_name</i>
Helvetica bold	Commands that you select from a menu	File → Open
	Keyboard shortcuts	Ctrl+C
<i>Italic font</i>	Variables in a syntax statement for which you must supply values	ngdbuild <i>design_name</i>
	References to other manuals	See the <i>Development System Reference Guide</i> for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected.
Square brackets []	An optional entry or parameter. However, in bus specifications, such as bus[7:0] , they are required.	ngdbuild [<i>option_name</i>] <i>design_name</i>
Braces { }	A list of items from which you must choose one or more	lowpwr = { on off }
Vertical bar	Separates items in a list of choices	lowpwr = { on off }
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	allow block <i>block_name</i> <i>loc1 loc2 ... locn</i> ;

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current file or in another file in the current document	See the section “ Additional Resources ” for details. Refer to “ Title Formats ” in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the <i>Virtex-II Handbook</i> .
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Getting Started with the ML300

1 Introduction

Getting Started with the ML300 provides an overview of the contents of the ML300 Evaluation Platform, directions on how to start using your ML300, and references to more information.

2 Contents

The ML300 Evaluation Platform comes to you in a jewel box with four draws and two documentation slots. Each of these drawers and slots contains a different aspect of the ML300 System.

2.1 ML300 Hardware Platform

In the bottom most drawer of the jewel box is the ML300 Hardware Platform drawer. This drawer contains the ML300 Hardware Platform with its associated power supply. The ML300 Hardware Platform is a full featured system that allows for demonstrating a wide variety of the capabilities of the Virtex-II Pro™ family of chips, as well as development of custom hardware and applications.

2.2 ML300 Software and IBM Microdrive

Included in the software drawer is all the software that you will need to get started with the ML300. This includes tools for developing IP, system generation, hardware and software debugging, and cores of system peripherals. The software is included in a CD Wallet and consists of nine CDs:

- Virtex-II Pro ML300 Evaluation Platform CD 1 - PC Install for ML300
- Virtex-II Pro ML300 Evaluation Platform CD 2 - Solaris Install for ML300
- Virtex-II Pro ML300 Evaluation Platform CD 3 - Linux Install for ML300
- Virtex-II Pro ML300 Evaluation Platform CD 4 - Linux PPC Install for ML300
- Virtex-II Pro ML300 Evaluation Platform CD 5 - IBM Microdrive™ Restoration for ML300
- Virtex-II Pro ML300 Evaluation Platform CD 6 - Schematics and PCB source files for ML300
- ISE 5.1i - Disk 1 of 2, Design Environment and Documentation - PC Evaluation Version
- ISE 5.1i - Disk 2 of 2, Device Files
- HDL Designer's Guide for Xilinx ISE 5.1i

On the back of the CD wallet is your registration ID that you will need to get started with the installation of the software. For details of how to use the registration ID, see the printed Installation Instructions document that is shipped with the kit.

Also included in this drawer is a gigabyte IBM Microdrive™ has been included with the ML300 Evaluation Platform. The Microdrive has been provided to serve two purposes:

- Most importantly, it serves as non-volatile storage for a variety of bitstreams for configuring the Virtex-II Pro using System ACE
- Additionally, it serves as a file system for the system when one is needed, such as when booting Linux.

2.3 ML300 Cables

The ML300 Evaluation Platform is shipped with a wide range of cables to provide for exploring all of the capabilities of the Virtex-II Pro devices, from a standard serial port connection for terminal access, to gigabit Ethernet over Fiber, to 3.125 gb/s over copper. The cables included are:

- 2 Serial port cables
- 2 Gigabit ethernet fiber-optic cables
- 1 HSSDC2/Infiniband cable
- 1 Serial ATA cable
- 1 Parallel port cable
- 1 IEEE-1394 (Firewire) cable
- 1 Set of board-to-board cables
- 1 Ethernet cable and 1 crossover Ethernet cable

2.4 Parallel Cable IV

A Parallel Cable IV cable has been included in the ML300 Evaluation Platform. The Parallel Cable IV cable serves a variety of purposes, including:

- Downloading hardware configurations to the Virtex-II Pro device
- Software download into the Power PC in the Virtex-II Pro device
- Hardware debug using Chip Scope Pro software tools
- Software debug using GNU Debugger (GDB)

2.5 Documentation

In the two slots provided for documentation in the ML300 jewel box, there is a Virtex-II Pro databook and a ML300 binder. There is additional documentation available on the CDs discussed in [2.2 ML300 Software and IBM Microdrive](#).

3 Playing with Your ML300 Evaluation Platform

3.1 From the Start Menu (Windows)

To start exploring the ML300 Evaluation Platform in Windows, go to **Start** → **Program Files** → **ML300 Evaluation Platform**. There is a wide variety of options to explore in the ML300 Evaluation Platform, as shown in [Figure 1](#).

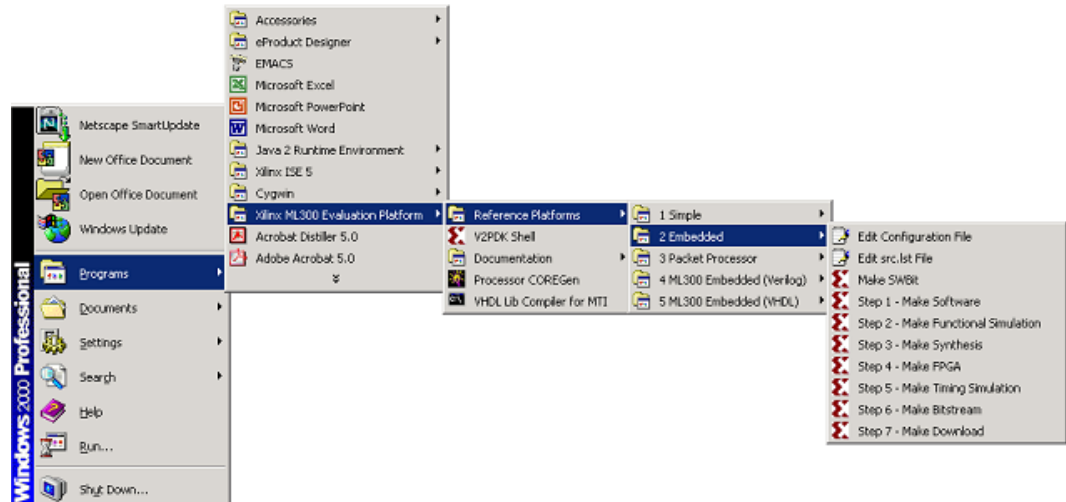


Figure 1: Start Menu for ML300 Evaluation Platform

From the main menu, you will see five options to choose from:

- Reference Platforms - Designs showing different uses of the Virtex-II Pro device
- V2PDK Shell - Command line for getting into the details
- Documentation - Links to ML300 and V2PDK documentation
- Processor COREGen - Ability to configure Cores for use with the Virtex-II Pro
- VHDL Lib Compiler for MTI - Compiles libraries for simulation when using VHDL

Within the Reference Platforms, there are five platforms to choose from:

- Simple - Including the Power PC with BRAM for memory and a UART for talking to the rest of the world.
- Embedded - A more complicated system, including a wide range of memory interfaces and peripherals. Basically a complete computer system.
- Packet Processor - Includes the Power PC and RocketIO multi-gigabit transceivers (MGTs)
- ML300 Embedded (Verilog) - Embedded design targeting the ML300 Hardware Platform, based in Verilog
- ML300 Embedded (VHDL) - Embedded design targeting the ML300 Hardware Platform, based in VHDL

For each of these, there are multiple options:

- Edit Configuration File - Controls the functioning of the different **make** functions, below. Controls device type, software to run on system, which simulator to use, which tool options to use, etc.
- Edit **src.lst** - An advanced user file, used to determine which files are used in a design, as well as determine which tools to call
- Make SWBit - Makes changes to the software included in an FPGA bitstream without needing to repeat the place and route of the entire FPGA
- Step 1 - Make Software - Compile the software selected in the configuration file
- Step 2 - Make Functional Simulation - Run a functional simulation on the design, using the selected software
- Step 3 - Make Synthesis - Synthesize the hardware design
- Step 4 - Make FPGA - Run the design through the implementation tools, ISE 5.1i
- Step 5 - Make Timing Simulation - Run a back-annotated timing simulation
- Step 6 - Make Bitstream - Make a bitstream for configuring the FPGA
- Step 7 - Make Download - Make a file for configuring the FPGA based upon the selected configuration method

3.2 From the Command Line (Windows and *nix)

Under Microsoft® Windows®, Solaris and Linux, the functionality of the ML300 Evaluation platform can be explored from the command line. From Windows, this takes the form of a V2PDK Shell (as mentioned in [3.1 From the Start Menu \(Windows\)](#)), while for Solaris and Linux, this takes the form of a standard console. From the command line, the same functionality is available as is discussed in the previous section, but reached in a different way.

From the ML300 install directory, the reference platforms can be seen in the platforms subdirectory. The documentation for the ML300 can be accessed from the docs subdirectory, which includes documentation of the ML300, the V2PDK and licensing information. Processor COREGen can be found in **proc_coregen** subdirectory.

In the platforms subdirectory, there are five directories corresponding to the five reference platforms. In each of these five directories, typing **make** will show a list of the options available for making a system, comparable to the Make Software, Make Functional Simulation, etc. discussed in the previous section. The **flow.cfg** file found in each of the subdirectories of platforms can be modified to control the configuration for each platform.

4 Exploring the Software Tools

4.1 Xilinx ISE 5.1i

An evaluation copy of Xilinx's ISE 5.1i is included as part of the ML300 Evaluation Platform. In addition to allowing exploration of the ISE 5.1i capabilities, inclusion of ISE 5.1i is required for full functionality of the V2PDK tools to create bitstreams and binaries to configure the Virtex-II Pro.

The ISE 5.1i tools can be accessed from the Start menu at **Start** → **Programs** → **Xilinx ISE5** → **Project Navigator**. More information can be found in ISE 5.1i documentation, or online at <http://www.xilinx.com/ise>.

4.2 ChipScope Pro 5.1i

A full version of ChipScope™ Pro 5.1i software is part of the ML300 Evaluation Platform. ChipScope Pro 5.1i is based on ChipScope ILA, which actually embeds a logic analyzer (ILA) in the internal logic of a Xilinx FPGA. ChipScope Pro extends the functionality of the basic ChipScope with an integrated bus analyzer (IBA) for use with the PLB and OPB buses of the PowerPC in the Virtex-II Pro. In addition, with the new Agilent trace core (ATC), ChipScope Pro 5.1i now interfaces directly to the Agilent FPGA Trace Port Analyzer, giving you deeper trace memory, faster clock speeds, more trigger options, all using fewer pins on the FPGA.

New in ChipScope Pro 5.1i:

- All of the capabilities of ChipScope ILA
- IBA Integrated Bus Analyzer core for IBM CoreConnect On-Chip Peripheral Bus
- Agilent Trace Core
- Support for the Agilent Trace Port Analyzer (sold separately)
- ChipScope Pro core generator - for inserting cores into HDL source
- ChipScope Pro core inserter - insert cores directly into the design netlist
- ChipScope Pro Analyzer Software - modify and view triggers, data sampling and waveform display

ChipScope Pro 5.1i software tools can be accessed from the Start menu at **Start** → **Programs** → **Chipscope Pro 5.1i**. More information can be found in ChipScope Pro 5.1i documentation, or online at <http://www.xilinx.com/chipscope>.

4.3 V2PDK

V2PDK is the Virtex-II Pro Platform FPGA Developer's Kit, and is included to provide an existing framework of hardware and software code to explore the capabilities of the Virtex-II Pro, as well as a basis to build new systems.

A wide variety of software and hardware tools are used to build a Virtex-II Pro design. The design flow is a tool chain that simplifies the design process by providing integration between the tools and automating tasks. The main focus of the design flow is integrating the programs with each other to accomplish the system design.

The system design process can be loosely divided into the following tasks:

- Builds the software application
- Simulates the hardware description
- Simulates the hardware with the software application
- Simulates the hardware into the FPGA using the software application in on-chip memory
- Runs timing simulation
- Configures the FPGA

4.4 GNU Tools

GNU software is used to develop software for the Virtex-II Pro family of FPGAs. This includes the GNU C compiler (GCC), the GNU binary utilities (**binutils**), the GNU debugger (GDB), and the GNU **make** program.

From the GNU Project website, <http://www.gnu.org>:

The GNU Project was launched in 1984 to develop a complete Unix-like operating system which is free software: the GNU system. (GNU is a recursive acronym for GNU's Not Unix; it is pronounced 'guh-NEW'.) Variants of the GNU operating system that use the Linux kernel are now widely used; though these systems are often referred to as "Linux," they are more accurately called GNU/Linux systems. As a prerequisite for the development of the GNU system, many different software packages-compilers, assemblers, linkers, debuggers, libraries, and other tools-had to be programmed.

5 Getting More Information

5.1 Printed Documentation

The printed documentation, as mentioned previously, takes the form of a Virtex-II Pro data book and an ML300 binder.

5.2 Electronic Documentation

Multiple documentation CDs have been included in the ML300 jewel box. Included on these CDs are:

- ML300 User Guide
- Virtex-II Pro Platform FPGA Developer's Kit

5.3 Online Documentation

Online documentation consists of two primary sites. There is a public access site that can be found on the Xilinx web site at <http://www.xilinx.com/ml300>. In addition, there is an ML300 lounge that provides additional information to purchasers of the ML300 Evaluation Platform.

The documentation on these two web pages includes all of the printed and electronic documentation provided with the ML300, plus updates and additional information.