

| REVISIONS |      |             |       |
|-----------|------|-------------|-------|
| DATE REV  | ZONE | DESCRIPTION | APPVD |
| 5/20/02   |      | NR          |       |

**I. DESCRIPTION:**

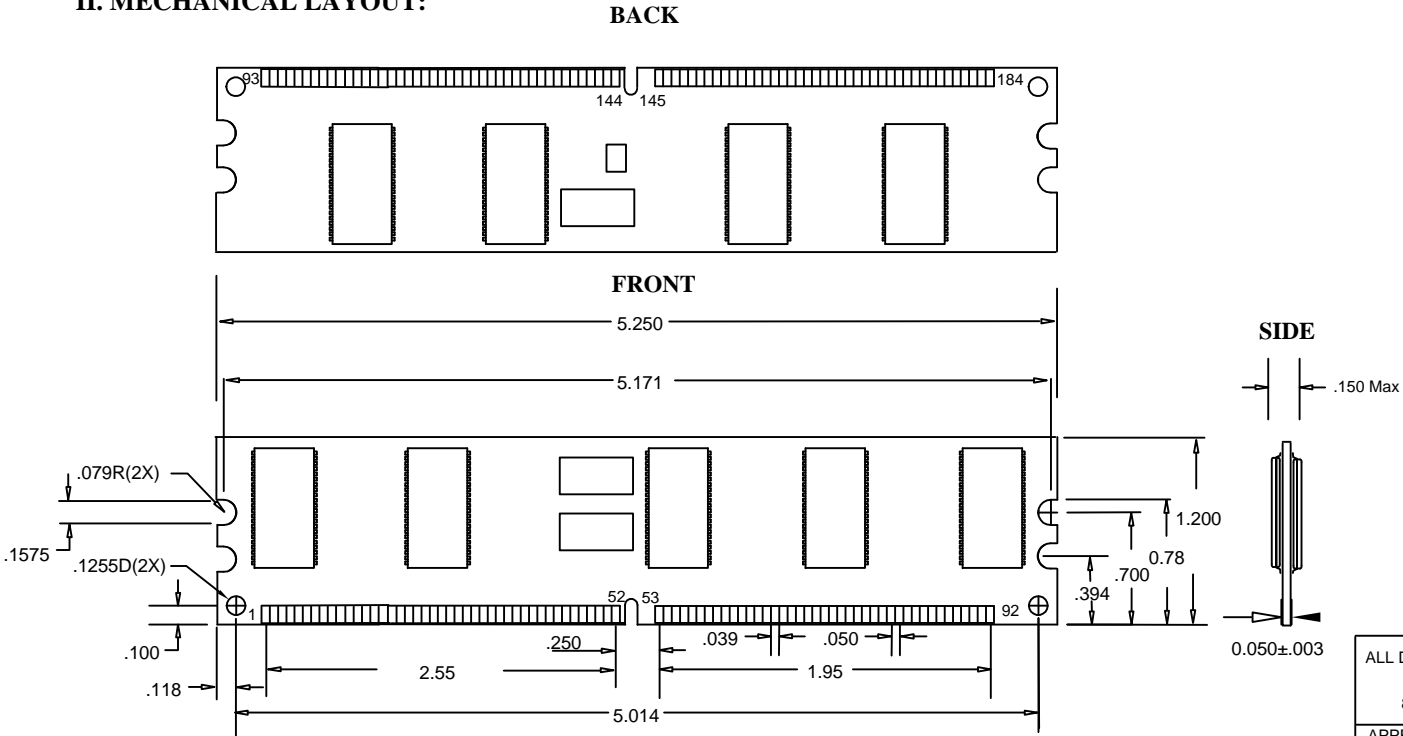
- W4F232726HA-5Q is a 32MX72 industry standard 184-pin low profile registered DDR400B-333 SDRAM DIMM for PC3200 (Intel compatible)
- Manufactured with 9 Infineon 32MX8 400-mil TSOPII-66 Double Data Rate Synchronous DRAM devices of 13- row, 10-column, and 4 -bank addressing.
- Organized as one logical rank, each rank is 32Mx72
- It requires 2.5V +/-0.2V power supply
- All inputs/outputs are compatible with SSTL\_2 interface
- Data Input/Output transaction on both edges of data strobe
- It supports auto (CBR) and self refresh modes, along with a power-saving power-down mode.
- It uses 8K refresh cycles in 64ms.
- It supports programmable Read/Write burst lengths of 2, 4, or 8
- Serial presence detect with EEPROM
- All contacts are gold plated

**III. TIMING:**

|                  | Allowable Operation Frequency (Max) |        |
|------------------|-------------------------------------|--------|
| Clock Cycle Time | CL=3*                               | CL=2.5 |
| 5 ns             | 200MHz                              | 166MHz |

Note:\* DDR400B @ CL=3

**II. MECHANICAL LAYOUT:**



Tolerances: +/- 0.005" unless otherwise specified

|                          |      |                                   |      |              |
|--------------------------|------|-----------------------------------|------|--------------|
| ALL DIMENSIONS IN INCHES |      | <b>WINTEC INDUSTRIES</b>          |      |              |
| 85616649/BRDA80A         |      | <b>32X72-5 DIMM SPECIFICATION</b> |      |              |
|                          |      | <b>W4F232726HA-5Q</b>             |      |              |
| APPROVALS                | DATE | SCALE                             | SIZE | DRAWINGS NO. |
| DRAW                     |      | NONE                              | A    |              |
| CHECKED                  |      |                                   |      |              |
| REV                      |      | DO NOT SCALE DRAWINGS             |      | SHEET 1 OF 5 |

#### IV. PINOUT:

Front side: A

| PIN# | SYMBOL  | PIN# | SYMBOL | PIN# | SYMBOL | PIN# | SYMBOL  |
|------|---------|------|--------|------|--------|------|---------|
| A1   | VREF    | A24  | DQ17   | A47  | DQS8   | A70  | Vcc     |
| A2   | DQ0     | A25  | DQS2   | A48  | A0     | A71  | NC      |
| A3   | Vss     | A26  | Vss    | A49  | CB2    | A72  | DQ48    |
| A4   | DQ1     | A27  | A9     | A50  | Vss    | A73  | DQ49    |
| A5   | DQS0    | A28  | DQ18   | A51  | CB3    | A74  | Vss     |
| A6   | DQ2     | A29  | A7     | A52  | BA1    | A75  | NC/CK2# |
| A7   | Vcc     | A30  | VccQ   | A53  | DQ32   | A76  | NC/CK2  |
| A8   | DQ3     | A31  | DQ19   | A54  | VccQ   | A77  | VccQ    |
| A9   | NC      | A32  | A5     | A55  | DQ33   | A78  | DQS6    |
| A10  | Reset#  | A33  | DQ24   | A56  | DQS4   | A79  | DQ50    |
| A11  | Vss     | A34  | Vss    | A57  | DQ34   | A80  | DQ51    |
| A12  | DQ8     | A35  | DQ25   | A58  | Vss    | A81  | Vss     |
| A13  | DQ9     | A36  | DQS3   | A59  | BA0    | A82  | VccID   |
| A14  | DQS1    | A37  | A4     | A60  | DQ35   | A83  | DQ56    |
| A15  | VccQ    | A38  | Vcc    | A61  | DQ40   | A84  | DQ57    |
| A16  | NC/CK1  | A39  | DQ26   | A62  | VccQ   | A85  | Vcc     |
| A17  | NC/CK1# | A40  | DQ27   | A63  | WE#    | A86  | DQS7    |
| A18  | Vss     | A41  | A2     | A64  | DQ41   | A87  | DQ58    |
| A19  | DQ10    | A42  | Vss    | A65  | CAS#   | A88  | DQ59    |
| A20  | DQ11    | A43  | A1     | A66  | Vss    | A89  | Vss     |
| A21  | CKE0    | A44  | CB0    | A67  | DQS5   | A90  | NC      |
| A22  | VccQ    | A45  | CB1    | A68  | DQ42   | A91  | SDA     |
| A23  | DQ16    | A46  | Vcc    | A69  | DQ43   | A92  | SCL     |

Back side: B

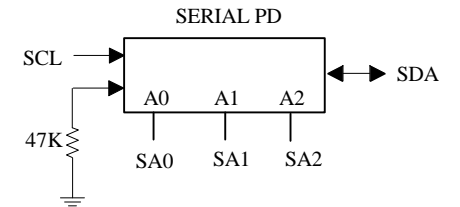
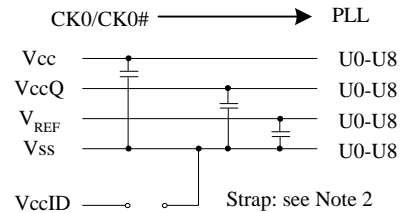
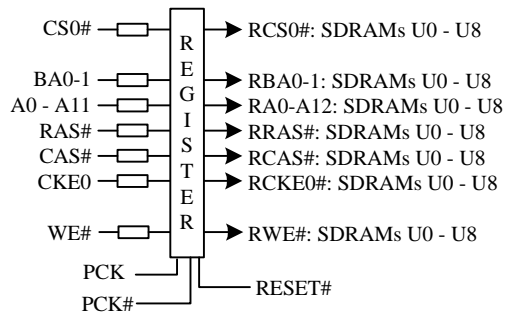
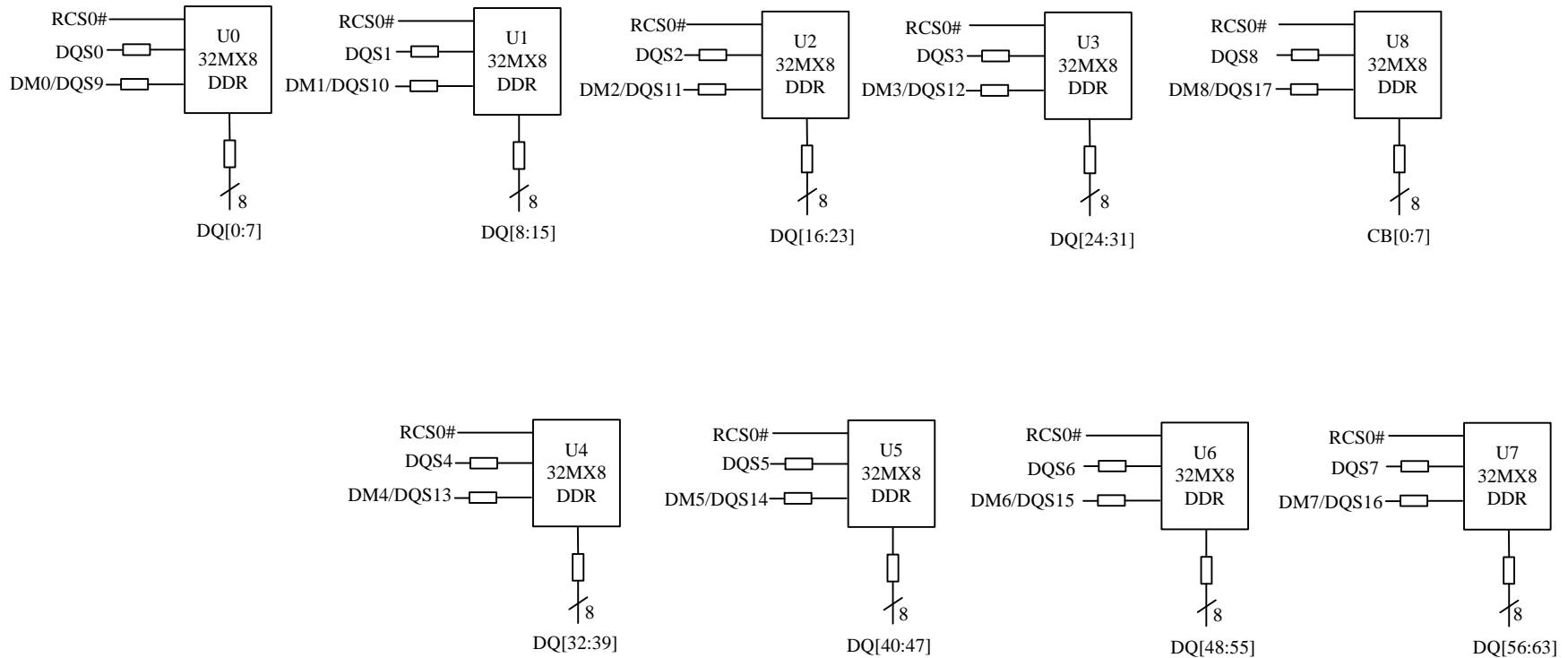
| PIN# | SYMBOL    | PIN# | SYMBOL    | PIN# | SYMBOL    | PIN# | SYMBOL    |
|------|-----------|------|-----------|------|-----------|------|-----------|
| B1   | Vss       | B24  | Vss       | B47  | Vss       | B70  | DQ47      |
| B2   | DQ4       | B25  | DQ21      | B48  | DM8/DQS17 | B71  | NC        |
| B3   | DQ5       | B26  | A11       | B49  | A10       | B72  | VccQ      |
| B4   | VccQ      | B27  | DM2/DQS11 | B50  | CB6       | B73  | DQ52      |
| B5   | DM0/DQS9  | B28  | Vcc       | B51  | VccQ      | B74  | DQ53      |
| B6   | DQ6       | B29  | DQ22      | B52  | CB7       | B75  | NC        |
| B7   | DQ7       | B30  | A8        | B53  | Vss       | B76  | Vcc       |
| B8   | Vss       | B31  | DQ23      | B54  | DQ36      | B77  | DM6/DQS15 |
| B9   | NC        | B32  | Vss       | B55  | DQ37      | B78  | DQ54      |
| B10  | NC        | B33  | A6        | B56  | Vss       | B79  | DQ55      |
| B11  | NC        | B34  | DQ28      | B57  | DM4/DQS13 | B80  | VccQ      |
| B12  | VccQ      | B35  | DQ29      | B58  | DQ38      | B81  | NC        |
| B13  | DQ12      | B36  | VccQ      | B59  | DQ39      | B82  | DQ60      |
| B14  | DQ13      | B37  | DM3/DQS12 | B60  | Vss       | B83  | DQ61      |
| B15  | DM1/DQS10 | B38  | A3        | B61  | DQ44      | B84  | Vss       |
| B16  | Vcc       | B39  | DQ30      | B62  | RAS#      | B85  | DM7/DQS16 |
| B17  | DQ14      | B40  | Vss       | B63  | DQ45      | B86  | DQ62      |
| B18  | DQ15      | B41  | DQ31      | B64  | VccQ      | B87  | DQ63      |
| B19  | NC        | B42  | CB4       | B65  | CS0#      | B88  | VccQ      |
| B20  | VccQ      | B43  | CB5       | B66  | NC        | B89  | SA0       |
| B21  | NC        | B44  | VccQ      | B67  | DM5/DQS14 | B90  | SA1       |
| B22  | DQ20      | B45  | CK0       | B68  | Vss       | B91  | SA2       |
| B23  | A12       | B46  | CK0#      | B69  | DQ46      | B92  | VccSPD    |

#### V. PIN NAMES:

| SYMBOL    | DESCRIPTION  | SYMBOL  | DESCRIPTION  | SYMBOL        | DESCRIPTION                      |
|-----------|--|---------|--|---------------|----------------------------------|
| A0-A12    | Address Inputs (Multiplexed)                             | VccQ    | Power Supply for DQ (2.5V+/-0.2V)                        | RAS#          | Row address Strobe               |
| BA0-BA1   | Bank Select Address                                      | Vss     | Ground   | CAS#          | Column Address Strobe            |
| DQ0-DQ63  | Data I/O   | VccSPD  | Serial EEPROM Power (2.5V-3.7V)                          | DM0-8/DQS9-17 | Low Data Masks/ High Data Strobe |
| DQS0-DQS8 | Data Strobe I/O  | SDA     | Serial Data I/O  | Vcc           | Power Supply (2.5V +/- 0.2V)     |
| CK0       | Clock Input (positive lines of three differential pairs) | SCL     | Serial clock   | VccID         | Vcc identification flag          |
| CKE0      | Clock Enable Input                                       | SA0-2   | Address in EEPROM  | Reset#        | Reset (Force Register Input low) |
| CS0#      | Chip select input  | CK0#    | Clock Input (negative lines of three differential pairs) | WE#           | Write enable                     |
| VREF      | SSTL_2 Reference Voltage for Inputs                      | CB0-CB7 | ECC check bits   | NC            | No connection                    |

|                          |      |                                   |      |              |
|--------------------------|------|-----------------------------------|------|--------------|
| ALL DIMENSIONS IN INCHES |      | <b>WINTEC INDUSTRIES</b>          |      |              |
|                          |      | <b>64X72-5 DIMM SPECIFICATION</b> |      |              |
|                          |      | <b>W4F232726HA-5Q</b>             |      |              |
| APPROVALS                | DATE | SCALE                             | SIZE | DRAWINGS NO. |
| DRAW                     |      | NONE                              | A    |              |
| CHECKED                  |      | DO NOT SCALE DRAWINGS             |      | SHEET 2 OF 5 |
| REV                      |      |                                   |      |              |

# FUNCTIONAL DIAGRAM



Note: 1. Address and control resistor values are 22 ohms.  
 2. DQ/DQS resistor values are 22 ohms.

3. VccID strap connections (for memory device Vcc, VccQ):  
 Strap Out (open): Vcc = VccQ  
 Strap In (Vss): Vcc ≠ VccQ

|                          |           |              |
|--------------------------|-----------|--------------|
| <b>WINTEC INDUSTRIES</b> |           |              |
| SPECIFICATION            |           |              |
| <b>W4F232726HA-5Q</b>    |           |              |
| SCALE<br>NONE            | SIZE<br>A | DRAWINGS NO. |
| DO NOT SCALE DRAWINGS    |           | SHEET 3 OF 5 |

## Absolute Maximum Ratings

| Item   | Ratings      | Unit |
|--|--------------|------|
| Voltage on any pin relative to V <sub>SS</sub> | -0.5 to +3.6 | V    |
| Power Dissipation                              | 12           | W    |
| Operating Temperature                          | 0 to +70     | °C   |
| Storage Temperature                            | -55 to +150  | °C   |
| Short Circuit Output Current                   | 50           | mA   |

## Recommended DC Operating Conditions

(T<sub>A</sub> = 0 to +70 °C)

| Parameter          | Symbol          | Min  | Typ | Max  | Unit |
|--------------------|-----------------|------|-----|------|------|
| Supply Voltage     | V <sub>CC</sub> | 2.3  | 2.5 | 2.7  | V    |
| Ground             | V <sub>SS</sub> | 0    | 0   | 0    | V    |
| Input High Voltage | V <sub>IH</sub> | 1.33 | -   | 3.0  | V    |
| Input Low Voltage  | V <sub>IL</sub> | -0.3 | -   | 0.97 | V    |

## DC Characteristics

(V<sub>CC</sub> = 2.5V±0.125V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to +70°C)

| Parameter   | Symbol            | Test Conditions   | Min  | Max  | Unit | Note |
|---|-------------------|---|--|------|------|------|
| Operating Current (One Bank Active)                 | I <sub>CC1</sub>  | Burst Lenth=2 t <sub>RC</sub> =t <sub>RCmin</sub> I <sub>OL</sub> = 0 mA  | -  | 1125 | mA   | 1    |
| Precharge Standby Current<br>In power-down mode     | I <sub>CC2P</sub> | CKE ≤ V <sub>IL(max)</sub><br>t <sub>CC</sub> = 10 ns   | -  | 81   | mA   |      |
| Precharge Standby Current<br>In non power-down mode | I <sub>CC2</sub>  | CS# = V <sub>IH</sub> (min.), CKE ≥ V <sub>IH</sub> (min) Input signals are changed once during 20ns<br>t <sub>CC</sub> = 10 ns | -  | 504  | mA   |      |
| No Operating Current                                | I <sub>CC3</sub>  | t <sub>CK</sub> = min., CS# = V <sub>IH</sub> (min), active state (max. 4 banks)  | CKE > V <sub>IH</sub> (min.)                   | -    | 310  | mA   |
|   | I <sub>CC3P</sub> |   | CKE < V <sub>IL</sub> (max.) (Power down mode) | -    | 108  | mA   |
| Burst Operating Current                             | I <sub>CC4</sub>  | I <sub>OL</sub> = 0 mA Page Burst. All Banks activated t <sub>CCD</sub> = 2CKs  | -  | 1350 | mA   | 1    |
| Auto Refresh Current                                | I <sub>CC5</sub>  | t <sub>CK</sub> = min., Auto Refresh command cycling  | -  | 1800 | mA   |      |
| Self Refresh Current                                | I <sub>CC6</sub>  | Self Refresh Mode, CKE = 0.2V   | -  | 234  | mA   |      |
| Output logic high voltage                           | V <sub>OH</sub>   | I <sub>OH</sub> = -2mA  | 2.4  | -    | V    |      |
| Output logic low voltage                            | V <sub>OL</sub>   | I <sub>OL</sub> = 2mA   | -  | 0.4  | V    |      |
| Input leakage current                               | I <sub>IL</sub>   | 0V ≤ V <sub>in</sub> < V <sub>CCQ</sub> + 0.3V  | -5   | 5    | uA   |      |
| Output leakage current                              | I <sub>OL</sub>   | 0V < V <sub>out</sub> < V <sub>CCQ</sub> + 0.3V, Dout = Disable   | -5   | 5    | uA   |      |

Note: 1. Measured with outputs open.

## Capacitance

(T<sub>A</sub> = 25°C, V<sub>CC</sub> = 2.5V±0.2V, f = 100 MHz)

| Parameter   | Symbol          | Max. | Unit |
|---|-----------------|------|------|
| Input Capacitance (CK0-CK0#)                          | C <sub>11</sub> | 8    | pF   |
| Input Capacitance (A0-A12, BA0, BA1, RAS#, CAS#, WE#) | C <sub>12</sub> | 54   | pF   |
| Input Capacitance (CKE0)                              | C <sub>13</sub> | 54   | pF   |
| Input Capacitance (CS0#)                              | C <sub>14</sub> | 54   | pF   |
| Input Capacitance (DM0-DM7)                           | C <sub>15</sub> | 7    | pF   |
| I/O Capacitance (DQ0-DQ63, CB0-CB7)                   | C <sub>10</sub> | 8    | pF   |

**WINTEC INDUSTRIES**

SPECIFICATION

**W4F232726HA-5Q**

|               |           |              |
|---------------|-----------|--------------|
| SCALE<br>NONE | SIZE<br>A | DRAWINGS NO. |
|---------------|-----------|--------------|

DO NOT SCALE DRAWINGS SHEET 4 OF 5

**AC Characteristics** (Please refer to IC MFG. individual value)(T<sub>A</sub> = 0 to +70 °C, V<sub>cc</sub> = 2.6V±0.1V, V<sub>ccQ</sub> = 2.6V±0.1V, V<sub>ss</sub> = 0V)

| Parameter  | Symbol             | Min             | Max   | Unit | Note |   |
|--|--------------------|-----------------|-------|------|------|---|
| <b>Clock and Clock Enable</b>                              |                    |                 |       |      |      |   |
| Clock Cycle Time   | CAS# Latency =3    | t <sub>CK</sub> | 5     | 10   | ns   | 4 |
|  | CAS# Latency =2.5  |                 | 6     | 10   | ns   |   |
| Clock Frequency  | CAS# Latency =3    | t <sub>CK</sub> | 200   | 100  | MHz  |   |
|  | CAS# Latency =2.5  |                 | 133   | 100  | MHz  |   |
| Access window of DQs from CLK/CLK#                         | t <sub>AC</sub>    | -0.5            | +0.5  | ns   |      |   |
| DQ and DM input pulse width (for each input)               | t <sub>DIPW</sub>  | 1.75            | -     | ns   |      |   |
| DQS-DQ skew, DQS to last DQ valid                          | t <sub>DOSO</sub>  | -               | 0.4   | ns   | 4    |   |
| Active to precharge command                                | t <sub>RAS</sub>   | 40              | 70K   | ns   |      |   |
| Active to READ or WRITE delay                              | t <sub>RC</sub>    | 15              | -     | ns   |      |   |
| Row precharge time   | t <sub>RP</sub>    | 15              | -     | ns   |      |   |
| Row active to Row active delay                             | t <sub>RRD</sub>   | 10              | -     | ns   |      |   |
| Access window of DQS from CLK/CLK#                         | t <sub>DQSK</sub>  | -0.55           | 0.55  | ns   |      |   |
| Write Command to first DQS latching transition             | t <sub>DQSS</sub>  | 0.72            | 1.28  | CLK  |      |   |
| Data-out high impedance window from CLK/CLK#               | t <sub>HZ</sub>    | -               | +0.65 | ns   |      |   |
| Data-out low impedance window from CLK/CLK#                | t <sub>LZ</sub>    | -0.65           | +0.65 | ns   |      |   |
| Clock High Pulse Width                                     | t <sub>CH</sub>    | 0.45            | 0.55  | ns   |      |   |
| Clock Low Pulse Width                                      | t <sub>CL</sub>    | 0.45            | 0.55  | ns   |      |   |
| Refresh to Refresh command interval                        | t <sub>REFC</sub>  | -               | 7.8   | us   | 1    |   |
| Address and Control Input Setup/Hold Time (fast slew rate) | t <sub>IS</sub>    | 0.6             | -     | ns   |      |   |
| Address and Control Input Setup/Hold Time (slow slew rate) | t <sub>IH</sub>    | 0.6             | -     | ns   |      |   |
| Data In and DM Setup Time                                  | t <sub>DS</sub>    | 0.40            | -     | ns   |      |   |
| Data In and DM Hold Time                                   | t <sub>DH</sub>    | 0.40            | -     | ns   |      |   |
| Self Refresh exit to READ command                          | t <sub>XSRD</sub>  | 200             | -     | CLK  |      |   |
| Power down exit time                                       | t <sub>PDEX</sub>  | 10              | -     | ns   |      |   |
| Read preamble  | t <sub>RPRE</sub>  | 0.9             | 1.1   | CLK  |      |   |
| Read postamble   | t <sub>RPOST</sub> | 0.4             | 0.6   | CLK  |      |   |
| Terminating voltage delay to V <sub>cc</sub>               | t <sub>VTD</sub>   | 0               | 0     | ns   |      |   |
| DQS Write preamble   | t <sub>WP</sub>    | 0.25            | -     | CLK  |      |   |
| DQS Write preamble setup time                              | t <sub>WPRES</sub> | 0               | -     | ns   | 2    |   |
| DQS Write postamble  | t <sub>WPST</sub>  | 0.4             | 0.6   | CLK  | 3    |   |
| DQS Write recovery time                                    | t <sub>WR</sub>    | 15              | -     | ns   |      |   |

| Parameter                             | Symbol            | Min  | Max | Unit | Note |
|---------------------------------------|-------------------|------|-----|------|------|
| Internal WRITE to READ command delay  | t <sub>WTR</sub>  | 1    | -   | CLK  |      |
| DQS-in low level width                | t <sub>SIL</sub>  | 0.35 | -   | CLK  |      |
| DQS-in high level width               | t <sub>SIH</sub>  | 0.35 | -   | CLK  |      |
| Mode Register Set-up time             | t <sub>MRD</sub>  | 2    | -   | CLK  |      |
| Exit self refresh to non-read command | t <sub>XSNR</sub> | 75   | -   | ns   |      |

**Note:**

- Maximum burst refresh of 8
- The specific requirement is that DQS be valid (High or Low) on or before this CK edge. the case shown (DQS going from High\_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t<sub>DQSS</sub>.
- The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
- For registered DIMMs, t<sub>CL</sub> and t<sub>CH</sub> are >= 45% of the period including both the half period jitter of the PLL and the half period jitter due to crosstalk on the DIMM.

**WINTEC INDUSTRIES**

SPECIFICATION

**W4F232726HA-5Q**

|               |           |              |
|---------------|-----------|--------------|
| SCALE<br>NONE | SIZE<br>A | DRAWINGS NO. |
|---------------|-----------|--------------|

DO NOT SCALE DRAWINGS SHEET 5 OF 5