FEATURES

- Simultaneously Monitors Three Supplies
  LTC1326: 5V, 3.3V and ADJ
  LTC1326-2.5: 2.5V, 3.3V and ADJ
- Guaranteed Threshold Accuracy: ±0.75%
- Low Supply Current: 20μA
- Internal Reset Time Delay: 200ms
- Manual Push-Button Reset Input
- Active Low and Active High Reset Outputs
- Active Low “Soft” Reset Output
- Power Supply Glitch Immunity
- Guaranteed RESET for VCC3 ≥ 1V or VCC5 ≥ 1V or VCC25 ≥ 1V
- 8-Pin SO and MSOP Packages

APPLICATIONS

- Desktop Computers
- Notebook Computers
- Intelligent Instruments
- Portable Battery-Powered Equipment

DESCRIPTION

The LTC®1326/LTC1326-2.5 are triple supply monitors intended for systems with multiple supply voltages. They provide micropower operation, small size and high accuracy supply monitoring.

Tight 0.75% threshold accuracy and glitch immunity ensure reliable reset operation without false triggering. The 20μA typical supply current makes the LTC1326/LTC1326-2.5 ideal for power-conscious systems.

The RST output is guaranteed to be in the correct state for VCC3, VCC5 or VCC25 down to 1V. The LTC1326/LTC1326-2.5 can be configured to monitor one, two or three inputs, depending on system requirements.

A manual push-button reset input provides the ability to generate a very narrow “soft” reset pulse (100μs typ) or a 200ms reset pulse equivalent to a power-on reset. Both SRST and RST outputs are open-drain and can be OR-tied with other reset sources.

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**LTC1326/LTC1326-2.5**

**ABSOLUTE MAXIMUM RATINGS**
(Notes 1, 2)

**Terminal Voltage**
- \( V_{CC3}, V_{CC5}, V_{CCA} \) ................. -0.5V to 7V
- \( RST, SRST \) .................................... -0.5V to 7V
- \( RST \) ...................................... -0.5V to \((V_{CC3} + 0.3V)\)
- \( PBR \) .......................................................... -7V to 7V

**Operating Temperature Range**
- LTC1326C/LTC1326C-2.5....................... 0°C to 70°C
- LTC1326I/LTC1326I-2.5 ..................... -40°C to 85°C

**Storage Temperature Range** ............ -65°C to 150°C

**Lead Temperature (Soldering, 10 sec)......... 300°C**

**PACKAGE/ORDER INFORMATION**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TOP VIEW</th>
<th>ORDER NUMBER</th>
<th>MS8 PACKAGE 8-LEAD PLASTIC MSOP</th>
<th>T(<em>{J\text{MAX}}) = 125°C, (\theta</em>{JA} = 250°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC1326CMS8</td>
<td></td>
<td>LTC1326CMS8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTC1326IM5</td>
<td></td>
<td>LTC1326IM5</td>
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<tr>
<th>PART NUMBER</th>
<th>TOP VIEW</th>
<th>ORDER NUMBER</th>
<th>S8 PACKAGE 8-LEAD PLASTIC SO</th>
<th>T(<em>{J\text{MAX}}) = 125°C, (\theta</em>{JA} = 150°C/W)</th>
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<tr>
<td>LTC1326CS8</td>
<td></td>
<td>LTC1326CS8</td>
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<td></td>
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<tr>
<td>LTC1326IS8</td>
<td></td>
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<td></td>
<td></td>
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<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TOP VIEW</th>
<th>ORDER NUMBER</th>
<th>S8 PACKAGE 8-LEAD PLASTIC SO</th>
<th>T(<em>{J\text{MAX}}) = 125°C, (\theta</em>{JA} = 150°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC1326CS8-2.5</td>
<td></td>
<td>LTC1326CS8-2.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTC1326IMS8-2.5</td>
<td></td>
<td>LTC1326IMS8-2.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Consult factory for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**

The \(\bullet\) denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \(T_A = 25°C\). \(V_{CC3} = 3.3V\), \(V_{CC5} = 5V\) (for LTC1326), \(V_{CC25} = 2.5V\) (for LTC1326-2.5), \(V_{CCA} = V_{CC3}\), \(T_A = 25°C\) unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{RT3})</td>
<td>Reset Threshold (V_{CC3})</td>
<td>(0°C \leq T_A \leq 70°C) (\quad -40°C \leq T_A \leq 85°C)</td>
<td>3.094</td>
<td>3.118</td>
<td>3.135</td>
<td>V</td>
</tr>
<tr>
<td>(V_{RT5})</td>
<td>Reset Threshold (V_{CC5}) (LTC1326)</td>
<td>(0°C \leq T_A \leq 70°C) (\quad -40°C \leq T_A \leq 85°C)</td>
<td>4.687</td>
<td>4.725</td>
<td>4.750</td>
<td>V</td>
</tr>
<tr>
<td>(V_{RT25})</td>
<td>Reset Threshold (V_{CC25}) (LTC1326-2.5)</td>
<td>(0°C \leq T_A \leq 70°C) (\quad -40°C \leq T_A \leq 85°C)</td>
<td>2.344</td>
<td>2.363</td>
<td>2.375</td>
<td>V</td>
</tr>
<tr>
<td>(V_{RTA})</td>
<td>Reset Threshold (V_{CCA})</td>
<td>(0°C \leq T_A \leq 70°C) (\quad -40°C \leq T_A \leq 85°C)</td>
<td>0.992</td>
<td>1.000</td>
<td>1.007</td>
<td>V</td>
</tr>
<tr>
<td>(V_{CC})</td>
<td>(V_{CC3}) Operating Voltage</td>
<td>(RST) in Correct Logic State</td>
<td>1</td>
<td>7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(I_{VCC3})</td>
<td>(V_{CC3}) Supply Current</td>
<td>(PBR = V_{CC3})</td>
<td>20</td>
<td>40</td>
<td></td>
<td>(\mu A)</td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. $V_{CC3} = 3.3V$, $V_{CC5} = 5V$ (for LTC1326), $V_{CC25} = 2.5V$ (for LTC1326-2.5), $V_{CCA} = V_{CC3}$, $T_A = 25^\circ C$ unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{VCC5}$</td>
<td>$V_{CC5}$ Input Current (LTC1326)</td>
<td>$V_{CC5} = 5V$</td>
<td>●</td>
<td>4</td>
<td>7</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{VCC25}$</td>
<td>$V_{CC25}$ Input Current (LTC1326-2.5)</td>
<td>$V_{CC25} = 2.5V$</td>
<td>●</td>
<td>2.8</td>
<td>7</td>
<td>$\mu A$</td>
</tr>
</tbody>
</table>
| $I_{VCCA}$ | $V_{CCA}$ Input Current | $V_{CCA} = 1V$  
$0^\circ C \leq T_A \leq 70^\circ C$  
$-40^\circ C \leq T_A \leq 85^\circ C$ | ● | -5 | 0 | 5 | nA |
| $I_{RST}$ | Reset Pulse Width | RST Low with $10k\Omega$ Pull-Up to $V_{CC3}$  
$0^\circ C \leq T_A \leq 70^\circ C$  
$-40^\circ C \leq T_A \leq 85^\circ C$ | ● | 140 | 200 | 280 | ms |
| $I_{SRST}$ | Soft Reset Pulse Width | SRST Low with $10k\Omega$ Pull-Up to $V_{CC3}$ | ● | 140 | 200 | 300 | ms |
| $I_{UV}$ | $V_{CC}$ Undervoltage Detect to RST | $V_{CC5}$, $V_{CC3}$ or $V_{CCA}$ Less Than Reset Threshold $V_{RT}$ by More Than 1% | | &nbsp | &nbsp | 13 | $\mu s$ |
| $I_{PBR}$ | PBR Pull-Up Current | $PBR = 0V$  
$0^\circ C \leq T_A \leq 70^\circ C$  
$-40^\circ C \leq T_A \leq 85^\circ C$ | ● | 3 | 7 | 10 | $\mu A$ |
| $V_{IL}$ | PBR, RST Input Low Voltage | | | ● | 0.8 | | V |
| $V_{IH}$ | PBR, RST Input High Voltage | | | ● | 2 | | V |
| $t_{PW}$ | PBR Min Pulse Width | Deassertion of PBR Input to SRST Output (PBR Pulse Width = 1$\mu$s) | | ● | 40 | | ns |
| $t_{DB}$ | PBR Debounce | | | ● | 20 | 35 | ms |
| $I_{PB}$ | PBR Assertion Time for Transition from Soft to Hard Reset Mode | $PBR$ Held Less Than $V_{IL}$  
$0^\circ C \leq T_A \leq 70^\circ C$  
$-40^\circ C \leq T_A \leq 85^\circ C$ | ● | 1.4 | 2.0 | 2.8 | s |
| $V_{OL}$ | RST Output Voltage Low | $I_{SINK} = 5mA$ | | ● | 0.15 | 0.4 | V |
| | $I_{SINK} = 100mA$,  
$0^\circ C \leq T_A \leq 70^\circ C$ | $V_{CC3} = 1V$, $V_{CC5} = 0V$  
$V_{CC3} = 0V$, $V_{CC5} = 1V$  
$V_{CC3} = 1V$, $V_{CC5} = 1V$ | ● | 0.05 | 0.4 | V |
| | $I_{SINK} = 100mA$,  
$-40^\circ C \leq T_A \leq 85^\circ C$ | $V_{CC3} = 1.1V$, $V_{CC5} = 0V$  
$V_{CC3} = 0V$, $V_{CC5} = 1.1V$  
$V_{CC3} = 1.1V$, $V_{CC5} = 1.1V$ | ● | 0.05 | 0.4 | V |
| | $I_{SINK} = 100mA$,  
$0^\circ C \leq T_A \leq 70^\circ C$ | $V_{CC3} = 1V$, $V_{CC25} = 0V$  
$V_{CC3} = 0V$, $V_{CC25} = 1V$  
$V_{CC3} = 1V$, $V_{CC25} = 1V$ | ● | 0.05 | 0.4 | V |
| | $I_{SINK} = 100mA$,  
$-40^\circ C \leq T_A \leq 85^\circ C$ | $V_{CC3} = 1.1V$, $V_{CC25} = 0V$  
$V_{CC3} = 0V$, $V_{CC25} = 1.1V$  
$V_{CC3} = 1.1V$, $V_{CC25} = 1.1V$ | ● | 0.05 | 0.4 | V |
| $SRST$ Output Voltage Low | $I_{SINK} = 2.5mA$ | | | ● | 0.15 | 0.4 | V |
| $V_{DH}$ | RST Output Voltage High (Note 3) | $I_{SINK} = 100mA$,  
$0^\circ C \leq T_A \leq 70^\circ C$ | | ● | $V_{CC3} - 1$ | | V |
| $SRST$ Output Voltage High (Note 3) | $I_{SINK} = 100mA$,  
$0^\circ C \leq T_A \leq 70^\circ C$ | $V_{CC3} = 1V$, $V_{CC25} = 0V$  
$V_{CC3} = 0V$, $V_{CC25} = 1V$  
$V_{CC3} = 1V$, $V_{CC25} = 1V$ | ● | $V_{CC3} - 1$ | &nbsp | V |
| $I_{PLH}$ | Prop Delay RST to RST  
High Input to Low Output | $C_{RST} = 20\mu F$ | | &nbsp | 25 | &nbsp | ns |
| $I_{PLH}$ | Prop Delay RST to RST  
Low Input to High Output | $C_{RST} = 20\mu F$ | | &nbsp | 45 | &nbsp | ns |
### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ C \). LTC1326 Only \( V_{CC3} = 3.3V \), \( V_{CC5} = 5V \), \( V_{CCA} = V_{CC3} \), \( T_A = 25^\circ C \) unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
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<th>CONDITIONS</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OVR} )</td>
<td>( V_{CC5} ) Reset Override Voltage</td>
<td>Override ( V_{CC5} ) Ability to Assert RST (Note 4)</td>
<td>( V_{CC3} )</td>
<td>0.025</td>
<td>●</td>
<td>V</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** The output pins SRST and RST have weak internal pull-ups to \( V_{CC3} \) of 6\( \mu A \) typ. However, external pull-up resistors may be used when faster rise times are required.

**Note 4:** The \( V_{CC5} \) reset override voltage is valid for an operating range less than approximately 4.15V. Above this point the override is turned off and the \( V_{CC5} \) pin functions normally.

### TYPICAL PERFORMANCE CHARACTERISTICS

**\( I_{VCC3} \) vs Temperature**

**\( I_{VCC5} \) vs Temperature**

**\( I_{VCC25} \) vs Temperature**

**\( V_{CCA} \) Input Current vs Input Voltage**

**\( V_{CC5} \) Transient Immunity**

**\( V_{CC25} \) Transient Immunity**
**TYPICAL PERFORMANCE CHARACTERISTICS**

- **V_{CCA} Transient Immunity**
- **V_{CC3} Transient Immunity**
- **V_{CC5} Threshold Voltage vs Temperature (LTC1326)**
- **V_{CC5} Threshold Voltage vs Temperature (LTC1326)**
- **V_{CC3} Threshold Voltage vs Temperature**
- **V_{CC3} Threshold Voltage vs Temperature**
- **V_{CC5} Threshold Voltage vs Temperature**
- **V_{CC5} Threshold Voltage vs Temperature**
- **V_{CC5} Threshold Voltage vs Temperature**
- **Reset Pulse Width vs Temperature**
- **“Soft” Reset Pulse Width vs Temperature**
- **PBR Assertion Time to Reset vs Temperature**
**PIN FUNCTIONS**

**VCC3 (Pin 1):** 3.3V Sense Input and Power Supply Pin for the IC. Bypass to ground with ≥ 0.1μF ceramic capacitor.

**VCC5 (Pin 2) (LTC1326):** 5V Sense Input. Used as gate drive for the RST output FET when the voltage on VCC3 is less than the voltage on VCC5. If unused, it can be tied to VCC3 (see Dual and Single Supply Monitor Operation in the Applications Information section).

**VCC25 (Pin 2) (LTC1326-2.5):** 2.5V Sense Input. Used as gate drive for RST output FET when the voltage on VCC3 is less than the voltage on VCC25. If unused, it can be tied to VCC3.

**VCCA (Pin 3):** 1V Sense, High Impedance Input. Can be used as a logic input with a 1V threshold. If unused, it can be tied to either VCC3 or VCC25.

**GND (Pin 4):** Ground.

**RST (Pin 5):** Reset Logic Output. Active high CMOS logic output, drives high to VCC3, buffered complement of RST. An external pull-down on the RST pin will drive this pin high.

**ST (Pin 6):** Reset Logic Output. Active low, open-drain logic output with weak pull-up to VCC3. Can be pulled up greater than VCC3 when interfacing to 5V logic. Asserted when one or more of the supplies are below trip thresholds and held for 200ms after all supplies become valid. Also asserted after PBR is held low for more than 2 seconds and for an additional 200ms after PBR is released.

**SRST (Pin 7):** Soft Reset. Active low, open-drain logic output with weak pull-up to VCC3. Can be pulled up greater than VCC3 when interfacing to 5V logic. Asserted for 100μs after PBR is held low for less than 2 seconds and released.

**PBR (Pin 8):** Push-Button Reset. Active low logic input with weak pull-up to VCC3. Can be pulled up greater than VCC3 when interfacing to 5V logic. When asserted for less than 2 seconds, outputs a soft reset 100μs pulse on the SRST pin. When PBR is asserted for greater than 2 seconds, the RST output is forced low and remains low until 200ms after PBR is released.
The three internal precision voltage comparators have response times that are typically 13 µs. This slow response time helps prevent mistriggering due to transients on each of the \(V_{CC}\) inputs. The part’s ability to suppress transients can be improved by bypassing each of the \(V_{CC}\) inputs with a 0.1 µF capacitor to ground.

**Push-Button Reset**

The parts provide a push-button reset input pin. The \(PBR\) input has an internal pull-up current source to \(V_{CC3}\). If the \(PBR\) pin is not used it can be left floating.

When the \(PBR\) pin is pulled low for less than \(t_{PB} (\approx 2\text{ sec})\), a narrow (100 µs typ) soft reset pulse is generated on the \(SRST\) output pin after the button is released. The push-button circuitry contains an internal debounce counter which delays the output of the soft reset pulse by typically 20 ms. This pin can be OR-tied to the \(RST\) pin and issue what is called a “soft” reset. The \(SRST\) thereby resets the microprocessor without interrupting the DRAM refresh cycle. In this manner DRAM information remains undisturbed. Alternatively, \(SRST\) may be monitored by the processor to initiate a software-controlled reset.

When the \(PBR\) pin is held low for longer than \(t_{PB} (\approx 2\text{ sec})\), a standard reset is generated on the \(RST\) and \(RST\) pins. Once the 2 second period has elapsed, a reset signal is produced by the push-button logic, thereby clearing the reset counter. Once the button is released, the reset counter begins counting the reset period (200 ms nominal). Consequently, the reset outputs remain asserted for approximately 200 ms after the button is released.
During a supply induced reset condition, the ability of the PBR pin to force a soft reset condition on the SRST pin is disabled. In other words SRST will remain high. If the PBR pin is held low, both during and after a supply induced reset (low RST), the RST pin will remain low until 200ms after the PBR goes high.

Power Detect/Gate Drive

The LTC1326/LTC1326-2.5 for the most part are powered internally from the VCC3 pin. The exception is at the gate drive of the output FET on the RST pin. On the input to this FET is power detection circuitry used to detect and drive the gate from either the 3.3V input pin (VCC3) or the 5V input pin (VCC5) on the LTC1326 or the 2.5V input pin (VCC5) on the LTC1326-2.5. The gate drive is derived from the pin with the highest potential. This ensures the part pulls the RST pin low as soon as either input pin is ≥ 1V.

Dual and Single Supply Monitor Operation

The VCC3, VCC5 and VCCA inputs may be individually disabled by the following override techniques which allow the LTC1326 or LTC1326-2.5 to be used as a dual or single supply monitor.

LTC1326 Override Functions

The VCCA pin, if unused, can be tied to either VCC3 or VCC5. This is an obvious solution since the trip points for VCC3 and VCC5 will always be greater than the trip point for VCCA.

The VCC5 input trip point is disabled if its voltage is equal to the voltage on VCC3 ±25mV and the voltage on VCC5 is less than 4.15V. In this manner, the part will behave as a 3.3V monitor and the VCC5 reset will be disabled.

The VCC5 trip point is reenabled when the voltage on VCC5 is equal to the voltage on VCC3 ±25mV and the two inputs are greater than approximately 4.15V. In this manner, the LTC1326 can function as a 5V monitor with the 3.3V monitor disabled.

When monitoring either 3.3V or 5V with VCC3 strapped to VCC5 (see Figure 1), the LTC1326 determines which is the appropriate range. The LTC1326 handles this situation as shown in Figure 2. Above 1V and below VRT3, RST is held low. From VRT3 to approximately 4.15V, the LTC1326 assumes 3.3V supply monitoring and RST is deasserted. Above approximately 4.15V, the LTC1326 operates as a 5V monitor. In most systems, the 5V supply will pass through the 3.1V to 4.15V region in <200ms during power-up, and the RST output will behave as desired. Table 1 summarizes the state of RST and RST at various operating voltages with VCC3 = VCC5.

<table>
<thead>
<tr>
<th>INPUTS (VCC3 = VCC5 = VCC)</th>
<th>RST</th>
<th>RST</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V ≤ VCC ≤ 1V</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1V ≤ VCC ≤ VRT3</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>VRT3 ≤ VCC ≤ 4.15V</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4.15V ≤ VCC ≤ VRT5</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>VRT5 ≤ VCC</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 1

Figure 2. RST Voltage vs Supply Voltage
Figure 3 contains a simple circuit for 5V systems that can’t risk the RST output going high in the 3.1V to 4.15V range (possibly due to very slow rise time on the 5V supply). Diode D1 powers the LTC1326 while dropping 0.6V from the VCC5 pin to the VCC3 pin. This prevents the part’s internal override circuit from being activated. Without the override circuit active, the RST pin stays low until VCC5 reaches VRT5 = 4.725V (See Figure 4).

**Figure 3. LTC1326 Monitoring a Single 5V Supply. D1 Used to Avoid RST High Near 3.3V to 4V (See Figure 2).**

LTC1326-2.5 Override Functions

The VCCA pin, if unused, can be tied to either VCC3 or VCC25. This is an obvious solution since the trip points for VCC3 and VCC25 will always be greater than the trip point for VCCA. Likewise, the VCC25, if unused, can be tied to VCC3. VCC3 must always be used. Tying VCC3 to VCC25 and operating off of a 2.5V supply will result in the continuous assertion of RST.

**Figure 4. RST Output Voltage Characteristics of the Circuit in Figure 3**

Extending ESD Tolerance on the PBR Input Pin

The PBR pin is susceptible to ESD since it may be brought out to a front panel in normal applications. The ESD tolerance of this pin can be increased by adding a resistor in series with the PBR pin. A 10k resistor can increase the ESD tolerance of the PBR pin to approximately 10kV. The PBR’s internal pull-up current of 7μA typical means there is only 70mV (150mV max) dropped across the resistor. See Figure 5.

**Figure 5. Triple Supply Monitor (3.3V, 2.5V and Adjustable) with Extended ESD Tolerance**

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**LTC1326/LTC1326-2.5**

**APPLICATIONS INFORMATION**

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**Figure 4. RST Output Voltage Characteristics of the Circuit in Figure 3**
TYPICAL APPLICATIONS

Triple Supply Monitor (3.3V, 5V and Adjustable)

Dual Supply Monitor (3.3V and 5V, Defeat VCCA Input)

Dual Supply Monitor (3.3V or 5V Plus Adj)

Dual Supply Monitor (3.3V Plus Adj)

REFER TO LTC1326 OVERRIDE FUNCTIONS IN THE APPLICATIONS INFORMATION SECTION.
TYPICAL APPLICATIONS

SRST Tied to RST and OR-Tying Other Sources to RST to Generate Reset and Reset

Using $V_{CC}$ Tied to DC/DC Feedback Divider

Using the Short Pulse Width, Push-Button Soft Reset Feature to Initiate Hard Reset
TYPICAL APPLICATIONS

Monitoring a Negative Supply

\[ R_4 = (100k)(0.98)(V_{\text{TRIP}} + 0.55)(-1) \]

<table>
<thead>
<tr>
<th>SUPPLY</th>
<th>( V_{\text{TRIP}} )</th>
<th>( R_4 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>-5V</td>
<td>-4.6V</td>
<td>392k</td>
</tr>
<tr>
<td>-3.3V</td>
<td>-3V</td>
<td>237k</td>
</tr>
<tr>
<td>-12V</td>
<td>-10.8V</td>
<td>1M</td>
</tr>
</tbody>
</table>

Reset Valid for \( V_{\text{CC3}} \) Down to 0V

\[ \text{RST OUTPUT WITH 100k PULL-UP TO V}_{\text{CC3}} \]

\[ \text{RST OUTPUT WITHOUT 100k PULL-UP, 10M LOAD TO GND} \]
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

**DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE.

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE.
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE
Triple Supply Monitor with 3.3V and 5V System Resets

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GND
VCCA
RST
SRST
PBR
VCC5
VCC3
LTC1326
Q1 2N7002
R1
R2
10k
10k
10
8
7
6
5
4
3
2
1

ADJUSTABLE SUPPLY OR DC/DC FEEDBACK DIVIDER

3.3V
5V

TO 3.3V SYSTEM RESET
TO 5V SYSTEM RESET
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PART NUMBER | DESCRIPTION | COMMENTS |
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LTC690 | 5V Supply Monitor, Watchdog Timer and Battery Backup | 4.65V Threshold |
LTC694-3.3 | 3.3V Supply Monitor, Watchdog Timer and Battery Backup | 2.9V Threshold |
LTC699 | 5V Supply Monitor and Watchdog Timer | 4.65V Threshold |
LTC1443/LTC1444/LTC1445 | Micropower Quad Comparators with 1% Reference | LTC1443 has 1.182V Reference, LTC1444/LTC1445 have 1.221V Reference and Adjustable Hysteresis |
LTC1536 | Precision Triple Supply Monitor for PCI Applications | Meets PCI IFAIL Timing Specifications |
LTC1540 | Nanopower Comparator with 2% Reference | 1.182V Reference, 300mA Supply Current, 8-Pin MSOP |
LTC1726-2.5 | Micropower Triple Supply Monitor for 2.5V, 3.3V and ADJ | Adjustable RESET and Watchdog Time Outs |
LTC1726-5 | Micropower Triple Supply Monitor for 5V, 3.3V and ADJ | Adjustable RESET and Watchdog Time Outs |
LTC1727-2.5 | Micropower Triple Supply Monitor with Individual Outputs | 2.338V, 3.086V, 1V Thresholds (±1.5%) 2.5, 3.3V, ADJ |
LTC1727-5 | Micropower Triple Supply Monitor with Individual Outputs | 4.675V, 3.086V, 1V Thresholds (±1.5%) 5V, 3.3V, ADJ |
LTC1728-1.8 | Micropower Triple Supply Monitor in 5-Pin SOT-23 Package | 2.805V, 1.683V, 1V Thresholds (±1.5%) 3V, 1.8V, ADJ |
LTC1728-2.5 | Micropower Triple Supply Monitor in 5-Pin SOT-23 Package | 2.338V, 3.086V, 1V Thresholds (±1.5%) 2.5, 3.3V, ADJ |
LTC1728-5 | Micropower Triple Supply Monitor in 5-Pin SOT-23 Package | 4.675V, 3.086V, 1V Thresholds (±1.5%) 5V, 3.3V, ADJ |
LTC1985-1.8 | Micropower Triple Supply Monitor for 3V, 1.8V and ADJ | Push-Pull RESET Output, SOT-23 |