

SN74LVCC3245A

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS585K – NOVEMBER 1996 – REVISED AUGUST 2002

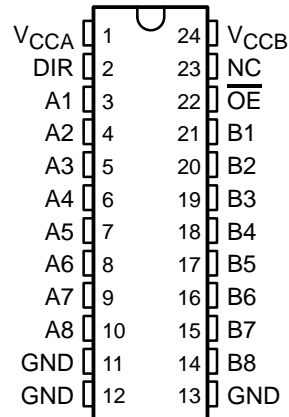
- Bidirectional Voltage Translator
- 2.3 V to 3.6 V on A Port and 3 V to 5.5 V on B Port
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track V_{CCB} , which accepts voltages from 3 V to 5.5 V, and the A port is designed to track V_{CCA} , which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, or from a 2.5-V to a 3.3-V system environment and vice versa.

The SN74LVCC3245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74LVCC3245ADW	LVCC3245A
		Tape and reel	SN74LVCC3245ADWR	
	SOP – NS	Tape and reel	SN74LVCC3245ANSR	LVCC3245A
	SSOP – DB	Tape and reel	SN74LVCC3245ADBR	LH245A
	TSSOP – PW	Tape and reel	SN74LVCC3245APWR	LH245A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each transceiver)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

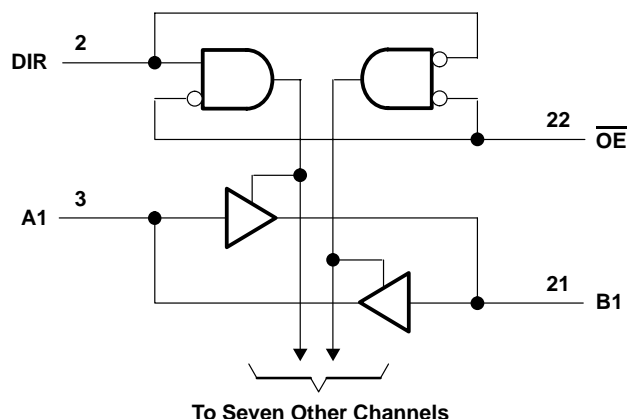
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB}	-0.5 V to 6 V
Input voltage range, V_I : All A ports (see Note 1)	-0.5 V to $V_{CCA} + 0.5$ V
All B ports (see Note 2)	-0.5 V to $V_{CCB} + 0.5$ V
Except I/O ports (see Note 1)	-0.5 V to $V_{CCA} + 0.5$ V
Output voltage range, V_O (see Note 2): All A ports	-0.5 V to $V_{CCA} + 0.5$ V
All B ports	-0.5 V to $V_{CCB} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O	± 50 mA
Continuous current through V_{CCA} , V_{CCB} , or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	63°C/W
DW package	46°C/W
NS package	65°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. This value is limited to 4.6 V maximum.
 2. This value is limited to 6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 4)

			V _{CCA}	V _{CCB}	MIN	NOM	MAX	UNIT
V _{CCA}	Supply voltage				2.3	3.3	3.6	V
V _{CCB}	Supply voltage				3	5	5.5	V
V _{IHA}	High-level input voltage	V _{OB} ≤ 0.1 V or V _{OB} ≥ V _{CCB} – 0.1 V	2.3 V	3 V	1.7			V
			2.7 V	3 V	2			
			3 V	3.6 V	2			
			3.6 V	5.5 V	2			
V _{IHB}	High-level input voltage	V _{OA} ≤ 0.1 V or V _{OA} ≥ V _{CCA} – 0.1 V	2.3 V	3 V	2			V
			2.7 V	3 V	2			
			3 V	3.6 V	2			
			3.6 V	5.5 V	3.85			
V _{ILA}	Low-level input voltage	V _{OB} ≤ 0.1 V or V _{OB} ≥ V _{CCB} – 0.1 V	2.3 V	3 V			0.7	V
			2.7 V	3 V			0.8	
			3 V	3.6 V			0.8	
			3.6 V	5.5 V			0.8	
V _{ILB}	Low-level input voltage	V _{OA} ≤ 0.1 V or V _{OA} ≥ V _{CCA} – 0.1 V	2.3 V	3 V			0.8	V
			2.7 V	3 V			0.8	
			3 V	3.6 V			0.8	
			3.6 V	5.5 V			1.65	
V _{IH}	High-level input voltage (control pins)	V _{OB} ≤ 0.1 V or V _{OB} ≥ V _{CCB} – 0.1 V	2.3 V	3 V	1.7			V
			2.7 V	3 V	2			
			3 V	3.6 V	2			
			3.6 V	5.5 V	2			
	V _{OA} ≤ 0.1 V or V _{OA} ≥ V _{CCA} – 0.1 V	2.3 V	3 V	2				
		2.7 V	3 V	2				
		3 V	3.6 V	2				
		3.6 V	5.5 V	2				
V _{IIL}	Low-level input voltage (control pins)	V _{OB} ≤ 0.1 V or V _{OB} ≥ V _{CCB} – 0.1 V	2.3 V	3 V			0.7	V
			2.7 V	3 V			0.8	
			3 V	3.6 V			0.8	
			3.6 V	5.5 V			0.8	
	V _{OA} ≤ 0.1 V or V _{OA} ≥ V _{CCA} – 0.1 V	2.3 V	3 V			0.8		
		2.7 V	3 V			0.8		
		3 V	3.6 V			0.8		
		3.6 V	5.5 V			0.8		
V _{IA}	Input voltage			0		V _{CCA}	V	
V _{IB}	Input voltage			0		V _{CCB}	V	
V _{OA}	Output voltage			0		V _{CCA}	V	
V _{OB}	Output voltage			0		V _{CCB}	V	

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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recommended operating conditions (see Note 4) (continued)

	V _{CCA}	V _{CCB}	MIN	NOM	MAX	UNIT
I _{OHA} High-level output current	2.3 V	3 V			-8	mA
	2.7 V	3 V			-12	
	3.3 V	3 V			-24	
I _{OHB} High-level output current	2.3 V	3.3 V			-12	mA
	2.7 V	3.3 V			-12	
	3.3 V	3 V			-24	
I _{OLA} Low-level output current	2.3 V	3 V			8	mA
	2.7 V	3 V			12	
	3.3 V	3 V			24	
I _{OLB} Low-level output current	2.3 V	3.3 V			12	mA
	2.7 V	3.3 V			12	
	3.3 V	3 V			24	
Δt/Δv Input transition rise or fall rate					10	ns/V
T _A Operating free-air temperature			-40		85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	UNIT
V _{OHA}		I _{OH} = -100 μA	3 V	3 V	2.9	3		V
		I _{OH} = -8 mA	2.3 V	3 V	2			
		I _{OH} = -12 mA	2.7 V	3 V	2.2	2.5		
			3 V	3 V	2.4	2.8		
		I _{OH} = -24 mA	3 V	3 V	2.2	2.6		
	2.7 V		4.5 V	2	2.3			
V _{OHB}		I _{OH} = -100 μA	3 V	3 V	2.9	3		V
		I _{OH} = -12 mA	2.3 V	3 V	2.4			
			2.7 V	3 V	2.4	2.8		
		I _{OH} = -24 mA	3 V	3 V	2.2	2.6		
	2.7 V		4.5 V	3.2	4.2			
V _{OLA}		I _{OL} = 100 μA	3 V	3 V			0.1	V
		I _{OL} = 8 mA	2.3 V	3 V			0.6	
		I _{OL} = 12 mA	2.7 V	3 V		0.1	0.5	
		I _{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
V _{OLB}		I _{OL} = 100 μA	3 V	3 V			0.1	V
		I _{OL} = 12 mA	2.3 V	3 V			0.4	
			3 V	3 V		0.2	0.5	
		I _{OL} = 24 mA	3 V	4.5 V		0.2	0.5	
I _I	Control inputs	V _I = V _{CCA} or GND	3.6 V	3.6 V 5.5 V		±0.1 ±0.1	±1 ±1	μA
I _{OZ} [†]	A or B ports	V _O = V _{CCA/B} or GND, V _I = V _{IL} or V _{IH}	3.6 V	3.6 V		±0.5	±5	μA
I _{CCA}	B to A	A port = V _{CCA} or GND, I _O = 0	3.6 V	Open		5	50	μA
		B port = V _{CCB} or GND, I _O = 0	3.6 V	3.6 V		5	50	
			5.5 V	5.5 V		5	50	
I _{CCB}	A to B	A port = V _{CCA} or GND, I _O = 0	3.6 V	3.6 V 5.5 V		5 8	50 80	μA
ΔI _{CCA} [‡]	A port	V _I = V _{CCA} - 0.6 V, Other inputs at V _{CCA} or GND, OE at GND and DIR at V _{CCA}	3.6 V	3.6 V		0.35	0.5	mA
	$\overline{\text{OE}}$	V _I = V _{CCA} - 0.6 V, Other inputs at V _{CCA} or GND, DIR at V _{CCA}	3.6 V	3.6 V		0.35	0.5	
	DIR	V _I = V _{CCA} - 0.6 V, Other inputs at V _{CCA} or GND, OE at GND	3.6 V	3.6 V		0.35	0.5	
ΔI _{CCB} [‡]	B port	V _I = V _{CCB} - 2.1 V, Other inputs at V _{CCB} or GND, OE at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C _i	Control inputs	V _I = V _{CCA} or GND	Open	Open		4		pF
C _{io}	A or B ports	V _O = V _{CCA/B} or GND	3.3 V	5 V		18.5		pF

[†] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[‡] This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V_{CC}.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}$, $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}$, $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A	B	1	9.4	1	6	1	7.1	ns
t_{PLH}			1	9.1	1	5.3	1	7.2	
t_{PHL}	B	A	1	11.2	1	5.8	1	6.4	ns
t_{PLH}			1	9.9	1	7	1	7.6	
t_{PZL}	\overline{OE}	A	1	14.5	1	9.2	1	9.7	ns
t_{PZH}			1	12.9	1	9.5	1	9.5	
t_{PZL}	\overline{OE}	B	1	13	1	8.1	1	9.2	ns
t_{PZH}			1	12.8	1	8.4	1	9.9	
t_{PLZ}	\overline{OE}	A	1	7.1	1	7	1	6.6	ns
t_{PHZ}			1	6.9	1	7.8	1	6.9	
t_{PLZ}	\overline{OE}	B	1	8.8	1	7.3	1	7.5	ns
t_{PHZ}			1	8.9	1	7	1	7.9	

operating characteristics, $V_{CCA} = 3.3\text{ V}$, $V_{CCB} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	$C_L = 50$, $f = 10\text{ MHz}$	38	pF
			Outputs enabled	
			4.5	
			Outputs disabled	

power-up considerations†

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems.

1. Connect ground before any supply voltage is applied.
2. Next, power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA} .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA} . Otherwise, keep DIR low.

† Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

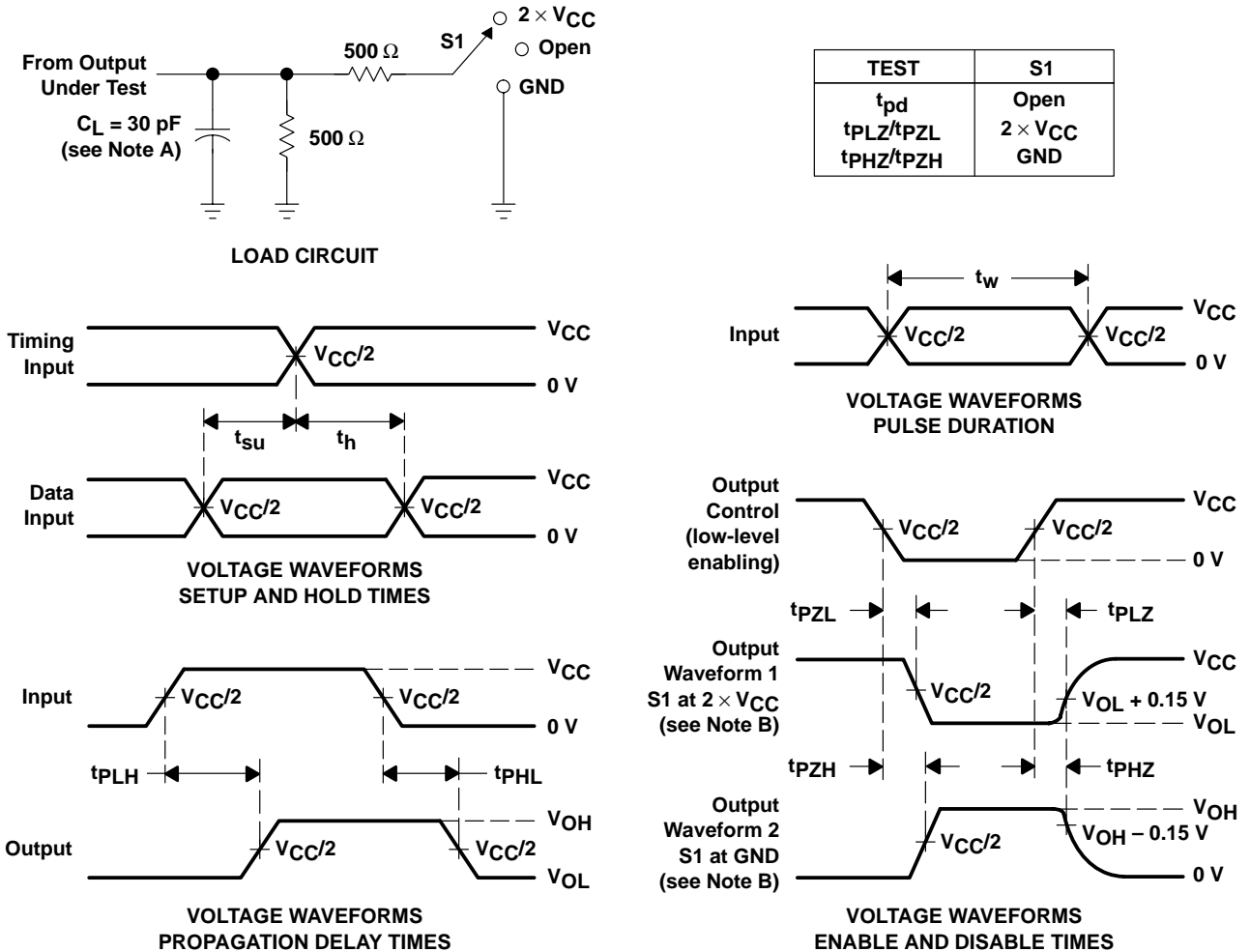


SN74LVCC3245A OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION FOR A PORT

$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ AND $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

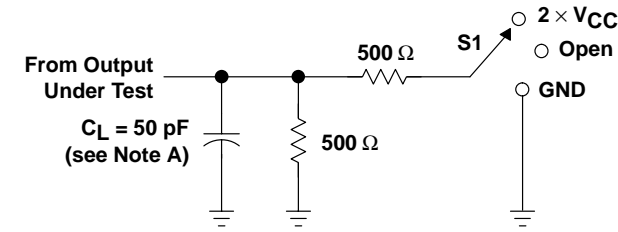
Figure 1. Load Circuit and Voltage Waveforms

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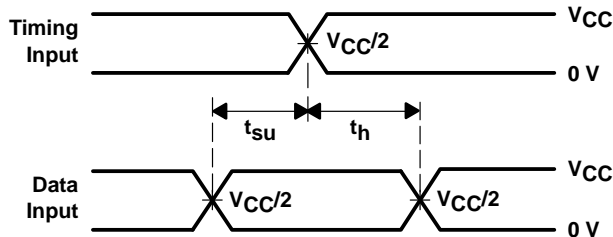
PARAMETER MEASUREMENT INFORMATION FOR B PORT

$$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V AND } V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$$

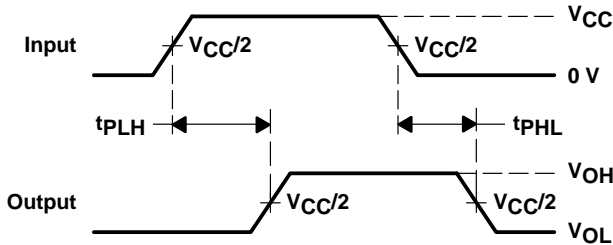


LOAD CIRCUIT

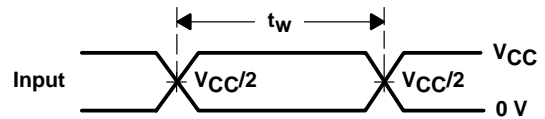
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 \times V_{CC}
t_{PHZ}/t_{PZH}	GND



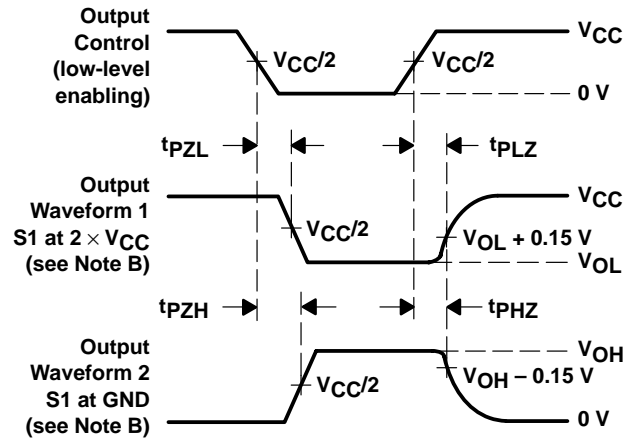
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

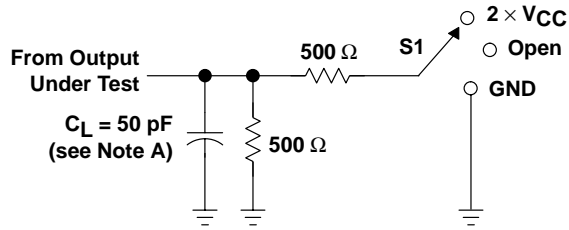
Figure 2. Load Circuit and Voltage Waveforms

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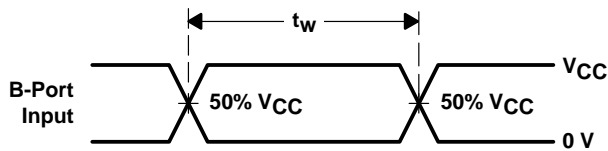
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PARAMETER MEASUREMENT INFORMATION FOR B PORT $V_{CCA} = 3.6\text{ V}$ AND $V_{CCB} = 5.5\text{ V}$

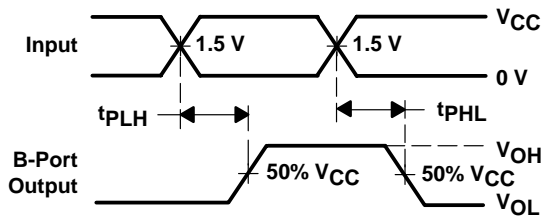


LOAD CIRCUIT

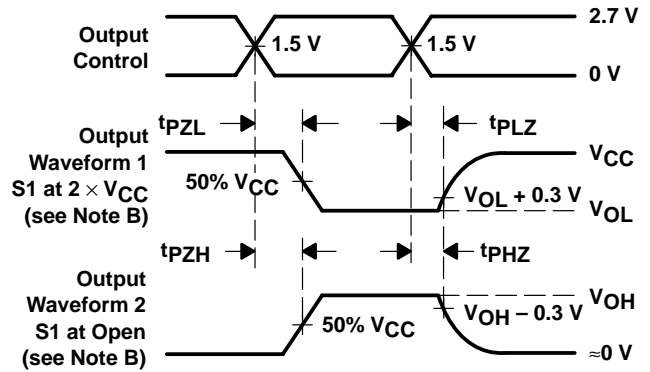
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

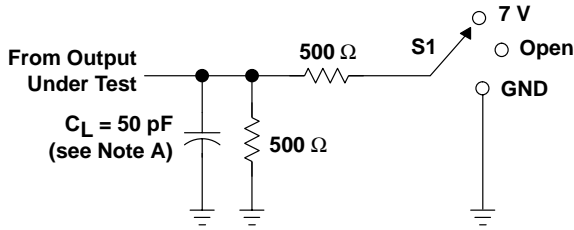
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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AND 3-STATE OUTPUTS

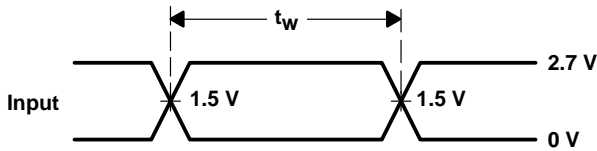
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PARAMETER MEASUREMENT INFORMATION FOR A AND B PORT
 V_{CCA} AND $V_{CCB} = 3.6\text{ V}$

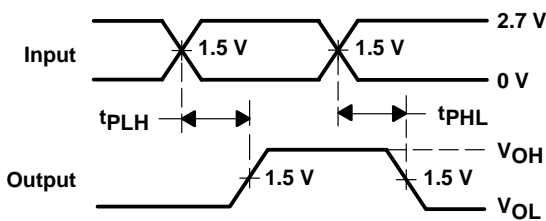


LOAD CIRCUIT

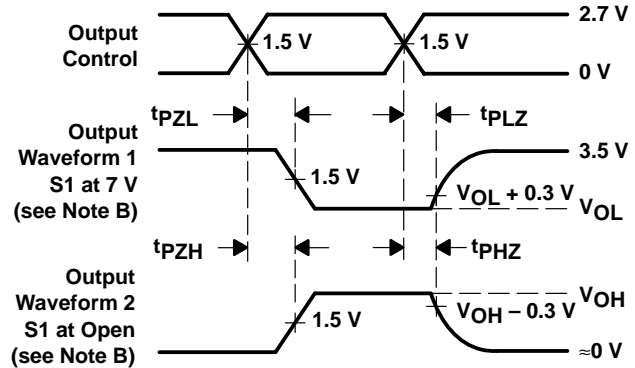
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

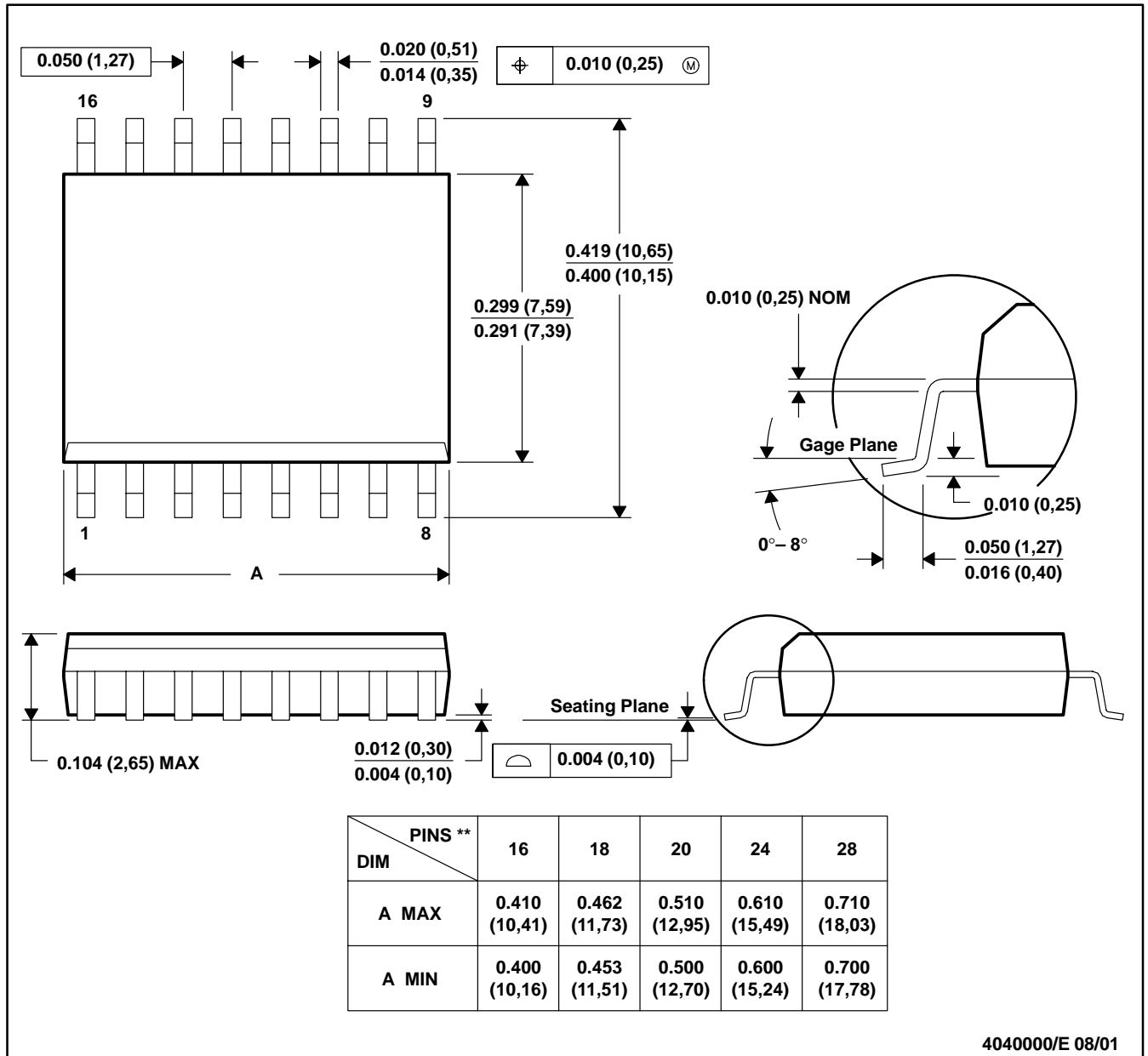
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN

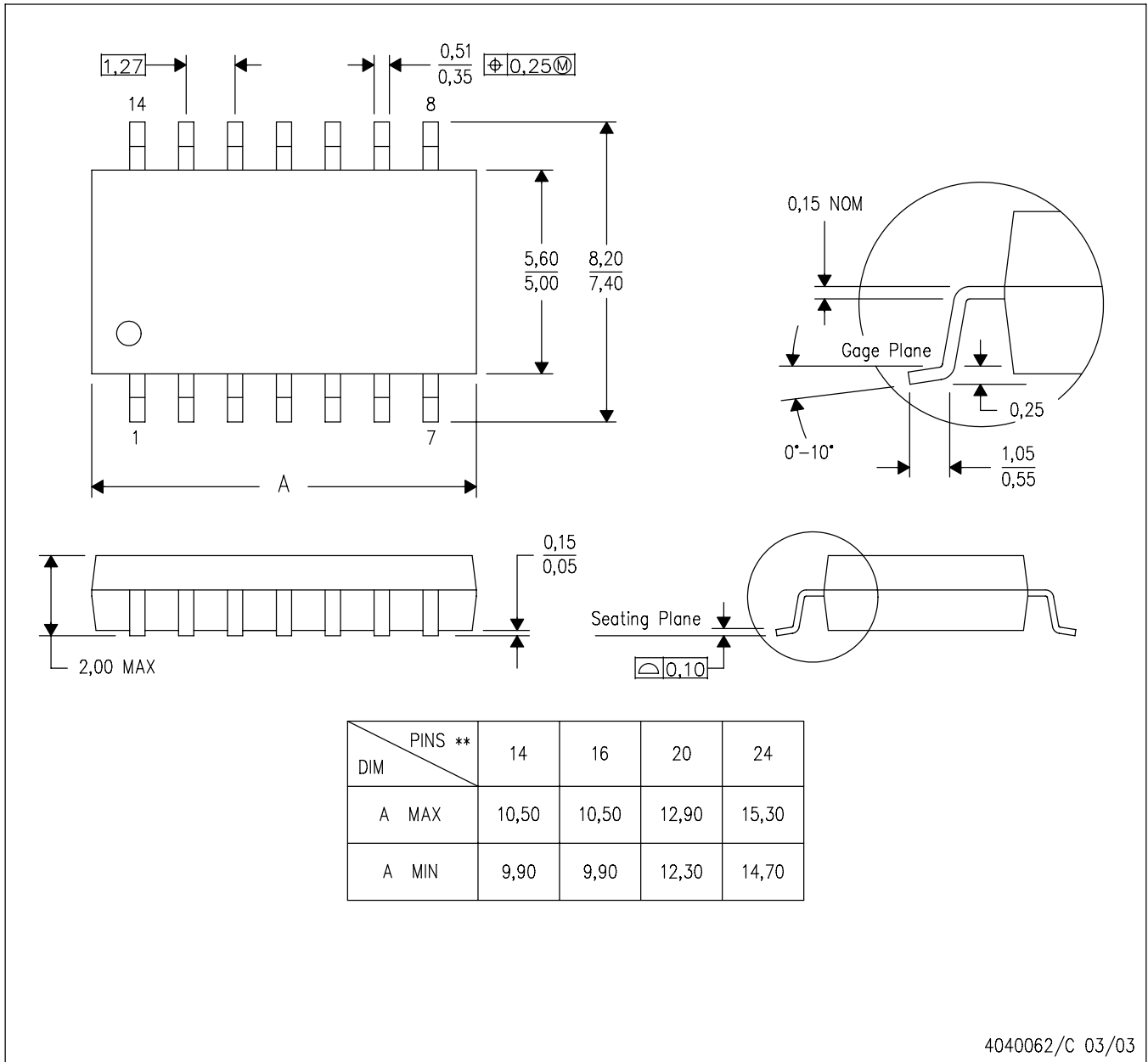


4040000/E 08/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

NS (R-PDSO-G**)
 14-PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

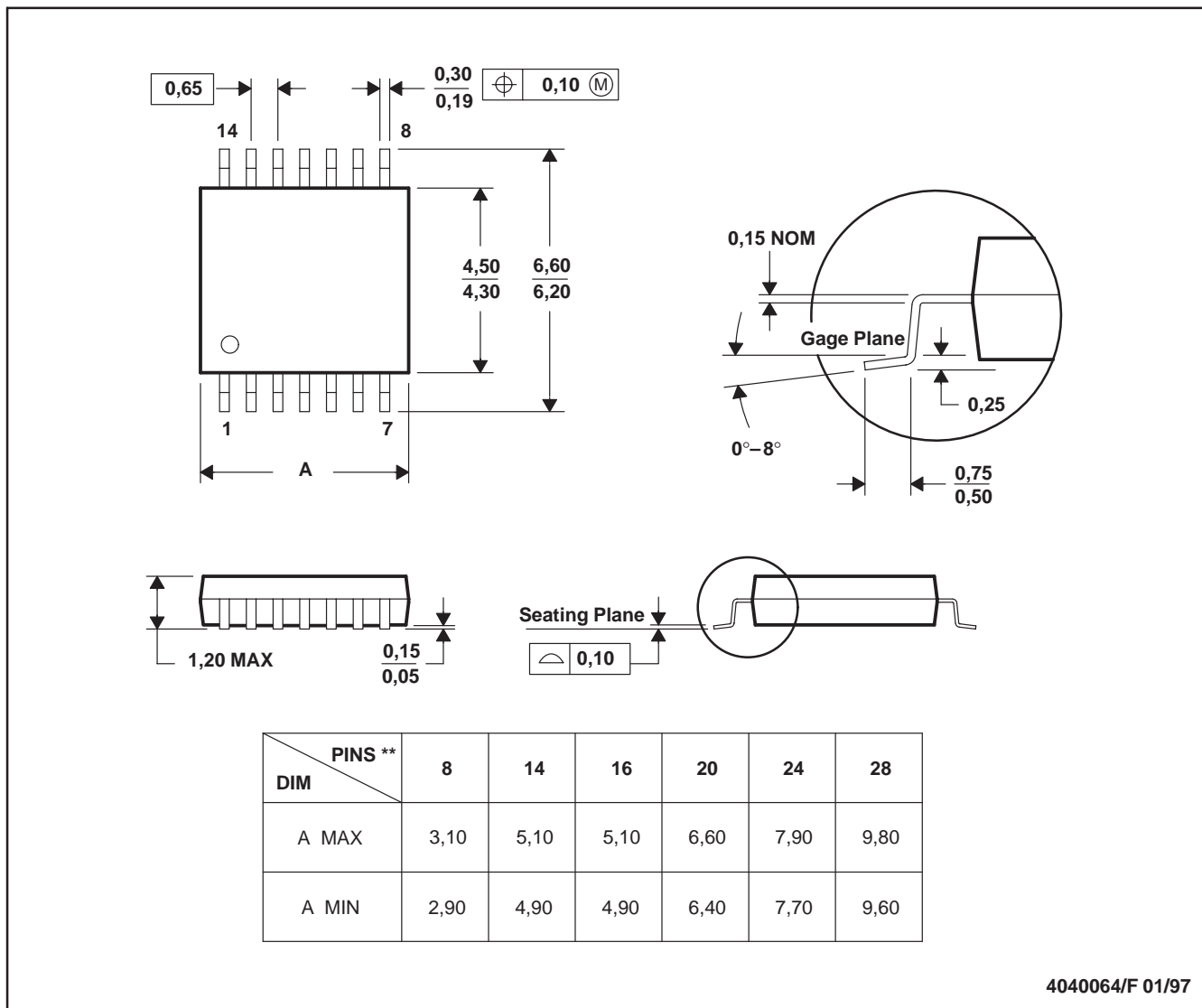


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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