ML501 Overview and Setup
Overview of the Hardware Designs and Software Applications
How to set up the equipment, software, CompactFlash, network, and terminal programs

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ML501 Overview

- ML501 Overview
- Equipment Overview
- Equipment Setup
- Software Setup
- CompactFlash Setup
- Network Setup
- Appendix

Note: This Presentation applies to the ML501
ML501 Overview

- The ML501 embedded development platform provides several reference designs and a versatile hardware platform for rapid prototyping and system verification.

- **Hardware Designs**
  - ml501_bsb_design
  - ml501_bsb_std_ip
  - ml501_std_ip_pcores

- **Software Applications**
  - Standalone non-OS application

*Note: Presentation applies to the ML501*
The ML501 MicroBlaze design hardware includes:

- DDR2 Interface (256 MB)
- BRAM
- External Memory Controller (EMC)
  - ZBT SRAM
- Networking
- UART
- Interrupt Controller
- System ACE CF Interface
- GPIO (IIC, LEDs and LCD)
- Timer
- PLB Arbiter

Note: Presentation applies to the ML501
Also Available From Xilinx

- These items are not included with the ML501, but are available for purchase from Xilinx:
  - Xilinx IDS (ISE Design Suite)
    - Includes ISE and XPS
  - Platform Cable USB
- These items are required to run the ML501 presentations

Note: Presentation applies to the ML501
ISE Software Requirement

- Xilinx ISE 11.1 software

Note: Presentation applies to the ML501
EDK Software Requirement

- Xilinx EDK 11.1 software

Note: Presentation applies to the ML501
ChipScope Software Requirements

- Xilinx ChipScope Pro 11.1 software

Note: Presentation applies to the ML501
ML501 Board

- Features the Xilinx Virtex™-5 XC5VLX50 FPGA

Note: Presentation applies to the ML501
ML501 Board

- Digital Video Connector
- Differential Clock Connectors
- SPDIF Out
- Piezo Speaker
- USB Host
- User Clock
- Virtex-5 XC5VLX50 FPGA
- Programming Interface
- Clock Chip, 25 MHz OSC
- LCD Interface Header
- System ACE CF Controller
- Xilinx Platform Flash
- Ethernet Port
- PS/2 Mouse and Keyboard Power Connector
- Power-On Switch, SW1
- Ethernet PHY
- USB Peripheral USB Host
- Microphone In
- Line In
- Amplified Line Out
- Line Out
- DDR2 SODIMM Memory
- Serial Port
- GPIO LEDs
- SYSACE Reset, PROG, CPU Reset Status & Error LEDs
- GPIO DIP SW
- SysACE Config, Mode Pins DIP SW
- XC95144XL CPLD (under Compact Flash)
- CompactFlash Slot
Equipment Overview

- **SiliconDrive™ 32 MB CompactFlash™**
  - Comes preloaded with hardware and software demonstration systems for ML501

*Note: Presentation applies to the ML501*
Equipment Overview

- **DVI monitor**
  - or

- **DVI to VGA adapter**
  - To connect from the ML501 DVI port to a standard VGA monitor
  - [http://www.belkin.com](http://www.belkin.com)

- **Pancake Fan (optional)**
  - Recommended for cooling the Virtex-5 device on the ML501 board

*Note: Presentation applies to the ML501*
Equipment Setup

- Set Front DIP Switches to 00010101 (1)

Note: Presentation applies to the ML501
ML501 Setup

- Set ML501 Jumper for GMII
  - Set both J40 to positions 1-2 (as shown)

Note: Presentation applies to the ML501
Equipment Setup

- User supplied – null modem serial cable

Note: Presentation applies to the ML501
Equipment Setup

- Connect Ethernet, DVI, and a USB Keyboard to ML501

Note: Presentation applies to the ML501
Software Setup

- Install a terminal program, such as Tera Term Pro
  - Required to input the commands, and view the results
- See the appendix for details on terminal programs and setup
CompactFlash Setup

- Insert the CompactFlash provided with the ML501 fully into the CompactFlash slot on the ML501 board

Note: Presentation applies to the ML501
Network Setup

- From the Windows Control Panel, open Network Connections
- Right-click on the Gigabit Ethernet Adapter and select Properties

**Note:** Presentation applies to the ML501
Network Setup

- Click Configure
  - Set the Media Type to Auto for 1 Gbps then click OK

Note: ML501 QuickStart uses 100Mb Full
Network Setup

- Reopen the properties after the last step
- Set your host (PC) to this IP Address:

![Local Area Connection Properties](image1)

![Internet Protocol (TCP/IP) Properties](image2)

**Note:** Some presentations use other IP addresses; change as directed.
Depending on your local network, the browser used for the LwIP demo may need the proxy disabled (Internet Explorer shown).

Note: Presentation applies to the ML501.
Appendix

- Terminal Program
- Creating Desktop Shortcuts

*Note: Presentation applies to the ML501*
Terminal Programs

- Terminal programs are used to communicate with the processor
- Terminal programs in this setup use a serial interface
- Free programs are available
  - Tera Term Pro (recommended)
    - [http://hp.vector.co.jp/authors/VA002416/teraterm.html](http://hp.vector.co.jp/authors/VA002416/teraterm.html)

**Note:** Presentation applies to the ML501
After installation, open Tera Term Pro and select the serial port desired.

Note: Presentation applies to the ML501
Select Setup → Serial Port...

Note: Presentation applies to the ML501
Tera Term Pro

- Set the serial port parameters
  - 9600 baud
  - 8 Data Bits
  - No Parity
  - One Stop Bit
  - No Flow Control

Note: Presentation applies to the ML501
Tera Term Pro

- Select Setup → Window...
  - Increase the Scroll Buffer to 10,000 lines

Note: Presentation applies to the ML501
Tera Term Pro

- **Select Setup → Save Setup…**
  - Save init file as COM1_9600.INI

**Note:** Presentation applies to the ML501
Repeat these steps for your second COM port

- Save init file as COM2_9600.INI

Note: Presentation applies to the ML501
Tera Term Pro

- **To automatically restore the command line options**
  - Use "/F=<file name>.ini"

- **To automatically open a log file**
  - Use "/L=<log file>.log"

**Note:** Presentation applies to the ML501
Tera Term Pro

- You can add shortcuts to your desktop for Tera Term Pro
  - Allows the command line options to be added here
- Right-click on your desktop and select New → Shortcut
- Browse for the terminal program folder

Note: Presentation applies to the ML501
For Tera Term Pro, link to the ttermpro.exe program file:

- C:\Program Files\TTERMPRO\ttermpro.exe

Note: Presentation applies to the ML501
Add the command line options

/F=COM1_9600.INI /L=COM1.LOG

Note: Presentation applies to the ML501
- Name the shortcut
- Click Finish

**Note:** Presentation applies to the ML501
References
ML501 Overview
http://www.xilinx.com/ml501
ML501 Getting Started Tutorial – UG227
ML501 Reference Design User Guide – UG228
ML501

- ML501 Schematics
- ML501 Bill of Material
  http://www.xilinx.com/support/documentation/boards_and_kits/ml505_501_bom.xls
Additional Documentation
Documentation

- **Virtex-5**
  - Silicon Devices
    http://www.xilinx.com/products/devices.htm
  - Virtex-5 Multi-Platform FPGA
  - Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms
    http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
  - Virtex-5 FPGA DC and Switching Characteristics Data Sheet
Documentation

- **Virtex-5**
  - Virtex-5 FPGA User Guide
  - Virtex-5 FPGA Configuration User Guide
  - Virtex-5 System Monitor User Guide
  - Virtex-5 Packaging and Pinout Specification
**Documentation**

- **Design Resources**
  - IDS - ISE Design Suite
  - ISE Manuals
  - ISE Command Line Tools User Guide
  - ISE Development System Libraries Guide


**Documentation**

- **Additional Design Resources**
  - Customer Support
    [http://www.xilinx.com/support](http://www.xilinx.com/support)
  - Xilinx Design Services:
  - Titanium Dedicated Engineering:
  - Education Services:
  - Xilinx On Board (Board and kit locator):
Documentation

- **Platform Studio**
  - Embedded Development Kit (EDK) Resources
  - EDK Concepts, Tools, and Techniques
Documentation

- **MicroBlaze**
  - MicroBlaze Processor
  - MicroBlaze Processor Reference Guide – UG081
Documentation

- **ChipScope Pro**
  - ChipScope Pro 11.1 ChipScope Pro Software and Cores User Guide
Documentation

- **Memory Solutions**
  - Demos on Demand – Memory Interface Solutions with Xilinx FPGAs
    http://www.demosondemand.com/clients/xilinx/001/page_new2/index.asp#35
  - Xilinx Memory Corner
    http://www.xilinx.com/products/design_resources/mem_corner
  - Additional Memory Resources
  - Xilinx Memory Interface Generator (MIG) 3.0 User Guide
  - Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator
Documentation

- **Ethernet**
  - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet
  - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide
  - Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide
  - LightWeight IP (lwIP) Application Examples – XAPP1026
- **PLB v4.6 IP**
  - Processor Local Bus (PLB) v4.6 – DS531
  - Multi-Port Memory Controller (MPMC) – DS643
  - XPS Multi-CChannel External Memory Controller (XPS MCH EMC) – DS575
  - XPS LocalLink TEMAC – DS537
PLB v4.6 IP

- XPS LocalLink FIFO – DS568
- XPS IIC Bus Interface – DS606
- XPS SYSACE (System ACE) Interface Controller – DS583
- XPS Timer/Counter – DS573
Documentation

- **PLB v4.6 IP**
  - XPS Interrupt Controller – DS572
  - Using and Creating Interrupt-Based Systems Application Note
  - XPS General Purpose Input/Output (GPIO) – DS569
  - XPS External Peripheral Controller (EPC) – DS581
Documentation

- PLB v4.6 IP
  - XPS 16550 UART – DS577
  - XPS Thin Film Transistor (TFT) Controller – DS695
  - XPS PS2 Controller – DS707
  - XPS Block RAM (BRAM) Interface Controller – DS596
    www.xilinx.com/support/documentation/ip_documentation/xps_bram_if_cntlr.pdf
- **OPB Bridge IP**
  - PLBV46 to OPB Bridge – DS403
  - On-Chip Peripheral Bus V2.0 with OPB Arbiter – DS401
Documentation

- **IP**
  - Local Memory Bus – DS445
  - Block RAM Block – DS444
  - Microprocessor Debug Module – DS641
  - LMB Block RAM Interface Controller – DS452
Documentation

- IP
  - JTAGPPC Controller – DS298
  - Processor System Reset Module – DS402
  - Clock Generator v2.0 – DS614
IP
- Utility Vector Logic – DS481
- Utility IO Multiplexer – DS694
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- ML501 Reference Design User Guide – UG228
**ML501**

- ML501 Schematics

- ML501 Bill of Material