ML505/506 MIG Design Creation
Using ISE™ 10.1i, MIG 2.1 and ChipScope™ Pro 10.1i

March 2008
Overview

• Hardware Setup
• Software Requirements
• CORE Generator™ software
  – Memory Interface Generator (MIG)
• Modify Design
  – Add ChipScope Pro Cores to Design
• Compile and Test Memory Interface

Note: This presentation applies to the ML505 and ML506
Virtex-5 DDR2 Capabilities

• MIG DDR2 SDRAM design supports frequencies up to 333 MHz
  – See MIG user guide
  – Answer Record AR29446 addresses MIG performance across device speed grades

• The ML505 ships with a –1 speed grade device
  – See the Virtex-5 Datasheet for a list of Virtex-5 supported memory interface speeds
Additional Setup Details

• Refer to ml505_overview_setup.ppt for details on:
  – Software Requirements
  – ML505/506 Board Setup
    • Equipment and Cables
    • Software
    • Network
  – Terminal Programs
    • This presentation requires the 9600-8-N-1 Baud terminal setup
Xilinx ML505 Board

Note: The ML506 uses an XC5VSX50T FPGA
ISE Software Requirement

- Xilinx ISE 10.1i software

Note: Presentation applies to the ML505 and ML506
Coregen Software Requirement

- Install Xilinx Coregen 10.1i

Note: Presentation applies to the ML505 and ML506
ChipScope Software Requirement

- Xilinx ChipScope Pro 10.1i

Note: Presentation applies to the ML505 and ML506
Setting Up the Hardware

• Connect the Xilinx Parallel Cable IV (PC4)
  – HW-PC4

• Optional - Pancake Fan
  – Recommended for keeping the Virtex™-5 device cool

Note: Presentation applies to the ML505 and ML506
Setting Up the Hardware

• SMA Cable
  – www.flrst.com
  – P/N: ASPI-024-ASPI-S402
Setting Up the Hardware

- Connect SMA Cables from J12/13 to J10/11
  - This will serve as the 200 MHz clock source for the memory controller

Note: Alternately, an external differential clock source can be connected to J10/11
Setting Up the Hardware

• Jumper J54 must be connected
  – This enables the output of the on-board ICS frequency source
Setting Up the Hardware

- Use SW6 to set the memory clock frequency
- Set SW6 to 200 MHz (1)
  - 200 MHz = 010 010 10 (Max memory clock frequency for a -1 speed grade)

Note: Presentation applies to the ML505 and ML506
CORE Generator

• Open the CORE Generator
  Start → All Programs → Xilinx ISE Design Suite 10.1i →
  ISE → Accessories → CORE Generator

• Create a new project; select File → New Project (1)

Note: Presentation applies to the ML505 and ML506
MIG Core Generation

• Create a project directory: ml505_mig_design
• Name the project: ml505_mig_design.cgp

• Set the Part (as shipped on the ML505):
  – Family: Virtex5
  – Device: xc5vlx50t
  – Package: ff1136
  – Speed Grade: -1

Note: For the ML506, set the part to xc5vsx50t
MIG Core Generation

- Set the Design Entry to Verilog
- Click OK

Note: Presentation applies to the ML505 and ML506
MIG Core Generation

- Right click on the MIG 2.1 and select Customize

Note: See Demos On Demand for an online tutorial on the use of MIG
MIG

- Click Next (1)

Note: Presentation applies to the ML505 and ML506
MIG

- Click Next (1)

Note: Presentation applies to the ML505 and ML506
• Click Next

Pin Compatible FPGAs

Pin Compatible FPGAs include all devices with the same package as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. **If you do not choose a Pin Compatible FPGA now and need to use a different FPGA later, the generated UCF may not work for the new device and a board spin may be required.**

To achieve maximum DDR2 performance, specific pin-outs may be required for memory controller designs that will be used with the PowerPC440 processor block in the FXT device. This includes Microblaze designs that will migrate to a PowerPC440 in an FXT device with a compatible package. These pin-outs are not provided through MIG but are part of the EDK install at: 

<EDK_INSTALL_LOCATION>/hw/XilinxProcessorIRlib/cores/ppc440mc_ddr2_v1_00_a/data/ppc440mc_ddr2.ucf.s

**Target FPGA**

| xc5vk50t-ff1136 |

<table>
<thead>
<tr>
<th>Pin Compatible FPGAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>xc5vfx85t-ff1136</td>
</tr>
<tr>
<td>xc5vfx110t-ff1136</td>
</tr>
<tr>
<td>xc5vfx155t-ff1136</td>
</tr>
<tr>
<td>xc5vfx70t-ff1136</td>
</tr>
<tr>
<td>xc5vfx100t-ff1136</td>
</tr>
<tr>
<td>xc5vfx130t-ff1136</td>
</tr>
<tr>
<td>xc5vsx50t-ff1136</td>
</tr>
<tr>
<td>xc5vsx95t-ff1136</td>
</tr>
</tbody>
</table>

**Note:** Presentation applies to the ML505 and ML506
MIG

• Click Next (1)

Note: Presentation applies to the ML505 and ML506
MIG

- MIG defaults to a maximum frequency of 266 for a Virtex-5 –1 speed grade selection
  – See AR29446
- Set the Memory Type to SODIMMs
- Set the Memory part to MT4HTF3264HY-53E
- Click Next

Note: Presentation applies to the ML505 and ML506
• Click Next on this screen

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• Click Next on this screen

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• Click Next on this screen

**Note:** Presentation applies to the ML505 and ML506
• Click Next on this screen

**MIG**

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**Reserve Pins**

Use this table to reserve pins that you do not want MIG to use. By default, MIG will use any available pin for the memory interface in the selected banks (next screen). The selections below allow you to reserve specific pins for other uses.

There is no need to reserve pins in banks you will not be selecting. The "Read UCF File" option reads in an existing UCF file to reserve pins already locked for other portions of the design. This option can be used instead of or in addition to manually reserving pins.

<table>
<thead>
<tr>
<th>Available Pins: 456</th>
<th>Reserved Pins: 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bank 1</td>
<td></td>
</tr>
<tr>
<td>Bank 2</td>
<td></td>
</tr>
<tr>
<td>Bank 3</td>
<td></td>
</tr>
<tr>
<td>Bank 4</td>
<td></td>
</tr>
<tr>
<td>Bank 11</td>
<td></td>
</tr>
<tr>
<td>Bank 12</td>
<td></td>
</tr>
<tr>
<td>Bank 13</td>
<td></td>
</tr>
<tr>
<td>Bank 15</td>
<td></td>
</tr>
<tr>
<td>Bank 17</td>
<td></td>
</tr>
<tr>
<td>Bank 18</td>
<td></td>
</tr>
<tr>
<td>Bank 19</td>
<td></td>
</tr>
<tr>
<td>Bank 20</td>
<td></td>
</tr>
<tr>
<td>Bank 21</td>
<td></td>
</tr>
<tr>
<td>Bank 22</td>
<td></td>
</tr>
</tbody>
</table>

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**Note:** Presentation applies to the ML505 and ML506
• Click Next on this screen

Note: Presentation applies to the ML505 and ML506
MIG

- Click Next on this screen

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Note: Presentation applies to the ML505 and ML506

Accept License Agreement (If you do not accept this agreement, the simulation output directory will not contain the memory model so you will need to acquire and configure a memory model appropriately).
MIG

- Click **Generate** (1)
- Close window after generation

Note: Presentation applies to the ML505 and ML506
MIG

- After the MIG core finishes generating, click OK on the Datasheet window

Note: Presentation applies to the ML505 and ML506
Design Modifications

• Add overlay files
  – ML505 specific UCF file as per Answer Record 29313
  – Pre-compiled ChipScope Pro design files used to validate the design

• Modify top level Verilog file
  – Support for ML505 Board as per AR 29313
  – Add ChipScope Pro to design
Add ML505 Files

- Unzip the `ml505_mig_design.overlay.zip` file
  - Unzip to the `ml505_mig_design` directory
  - See [ChipScope Pro documentation](#) for details on generating/instantiating the ICON and ILA cores

Note: ML506: `ml506_mig_design.overlay.zip`
Modify Design for ML505

• Open the top-level Verilog file, mig_21\example_design\rtl\ddr2_sdram.v
  – Change the DQ_IO_MS parameter:
    64'b10100101_10100101_10100101_10100101_10100101_10100101_10100101_10100101
    To:
    64'b01110101_00111101_00001111_00011110_00101110_11000011_11000001_10111100

Note: These changes are associated with AR 29313
Add ChipScope Pro

- Add these lines to the top-level Verilog file:
  
  wire [35:0] control;
  wire clk;
  wire [71:0] data;
  wire [7:0] trig0;

Note: Presentation applies to the ML505 and ML506
Add ChipScope Pro

- Add these lines to the top-level Verilog file before endmodule:

```verilog
icon i_icon
  (.control0(control))
);

ila i_ila
  (.control(control),
    .clk(clk0),
    .data(data),
    .trig0(trig0)
);
assign data[63:0] = app_af_addr;
assign data[64]   = app_wdf_afull;
assign data[65]   = app_af_afull;
assign data[66]   = app_wdf_wren;
assign data[67]   = app_af_cmd;
assign data[68]   = phy_init_done;
assign data[69]   = idelay_ctrl_rdy;
assign data[70]   = sys_RST_N;
assign data[71]   = error;
assign trig0[0]   = phy_init_done;
assign trig0[1]   = idelay_ctrl_rdy;
assign trig0[2]   = sys_RST_N;
assign trig0[3]   = error;
assign trig0[4]   = app_wdf_afull;
assign trig0[5]   = app_af_afull;
assign trig0[6]   = app_wdf_wren;
assign trig0[7]   = app_af_cmd;
```
Add ChipScope Pro

- Add these lines to the top-level Verilog file after endmodule:

```verilog
module icon
(
  control0
);
output [35:0] control0;
endmodule

module ila
(
  control, clk, data, trig0
);
input [35:0] control;
input clk;
input [71:0] data;
input [7:0] trig0;
endmodule
```
Generate Bitstream

- Start a windows command shell and enter these commands:
  ```
cd ml505_mig_design\mig_21\example_design\par
ise_flow.bat
  ```

Note: Presentation applies to the ML505 and ML506
ChipScope Pro Setup

- After the design compiles, open ChipScope Pro Analyzer
- Click on the Open Cable Button (1)
ChipScope Pro Setup

- Select Device → DEV:4 MyDevice4 (XC5VLX50T) → Configure…
- Select <Design Path>\mig_21\example_design\par\ddr2_sdram.bit
ChipScope Pro Setup

• Select File → Open Project…
• Select <Design Path>\mig_21\example_design\par\chipscope.cpj
ChipScope Pro Setup

- Click on Trigger Setup to view trigger settings
- The error bit value should be set to 1
ChipScope Pro Setup

- Click on Waveform
- Click the Arm Trigger button (1)
- Detection of an error will cause ChipScope Pro to trigger
ChipScope Pro Setup

- To force a trigger, in order to view the waveform, click the T! button (1)
ML505 DDR2 Verified at 200 MHz

- Virtex-5 –1 speed grade device supports 200 MHz DDR2 operation as stated in the Virtex-5 datasheet
- The ML505 SODIMM supports 200 MHz
  - Supplied DDR2 SODIMM is rated for 266 MHz operation
- The MIG test design and ChipScope Pro Analyzer verify operation of the ML505 with a Virtex-5 –1 speed grade device, at the specified clock rate of 200 MHz
Appendix
ML505 DDR2 at 266 MHz

- An external signal generator was used to clock the MIG test design on the ML505 at the maximum clock rate selectable in the MIG tool, 266 MHz
- Supplied DDR2 SODIMM is rated for 266 MHz operation
- The MIG test design and ChipScope Pro Analyzer verify operation of the ML505 at the maximum selectable MIG clock rate of 266 MHz for a -1 speed grade device
  - See AR29446
Documentation

• ML505/506
  – ML505 Overview
    http://www.xilinx.com/ml505
  – ML506 Overview
    http://www.xilinx.com/ml506
  – ML505/506 Getting Started Tutorial – UG348
  – ML505/506 Schematics
Documentation

• Virtex-5
  – Silicon Devices
    http://www.xilinx.com/products/silicon_solutions
  – Virtex-5 Multi-Platform FPGA
  – Virtex-5 Family Overview: LX, LXT, and SXT Platforms
    http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
  – Virtex-5 FPGA Configuration User Guide
  – Virtex-5 FPGA DC and Switching Characteristics Data Sheet
Documentation

• RocketIO
  – RocketIO GTP Transceivers
  – RocketIO GTP Transceiver User Guide
Documentation

• Design Resources
  – ISE Development Tools and IP
    http://www.xilinx.com/ise
  – Integrated Software Environment (ISE) Foundation Resources
    http://www.xilinx.com/ise/logic_design_prod/foundation.htm
  – ISE Manuals
    http://www.xilinx.com/support/software_manuals.htm
  – ISE Development System Reference Guide - 9.2i
    http://toolbox.xilinx.com/docsan/xilinx92/books/docs/dev/dev.pdf
Documentation

• Platform Studio
  – Embedded Development Kit (EDK) Resources
    http://www.xilinx.com/edk
  – MicroBlaze Processor Reference Guide – UG081
Documentation

• Additional Design Resources
  – Customer Support
    http://www.xilinx.com/support
  – Xilinx Design Services:
    http://www.xilinx.com/xds
  – Titanium Dedicated Engineering:
    http://www.xilinx.com/titanium
  – Education Services:
    http://www.xilinx.com/education
  – Xilinx On Board (Board and kit locator):
    http://www.xilinx.com/xob
Documentation

• Memory Solutions
  – Demos on Demand - Memory Interface Solutions with Xilinx FPGAs
    http://www.demosondemand.com/clients/xilinx/001/page/index.asp#memory
  – Xilinx Memory Corner
    http://www.xilinx.com/products/design_resources/mem_corner
  – Additional Memory Resources
  – Xilinx Memory Interface Generator (MiG) 2.0 User Guide
  – Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator
Documentation

• ChipScope Pro
  – ChipScope Pro 9.2i Serial IO Toolkit User Manual
    http://www.xilinx.com/ise/verification/chipscope_pro_siotk_9_2i Ug213.pdf
  – ChipScope Pro 9.2i ChipScope Pro Software and Cores User Guide
    http://www.xilinx.com/ise/verification/chipscope_pro_sw_cores_9_2i Ug029.pdf