



# ML505/506 Four GTPs IBERT Design Creation Using 10.1i SP3 ChipScope™ Pro

October 2008



# ML505 IBERT Overview

- Software Requirements
- Design Generation
  - Highlighting the Virtex-5 RocketIO™ GTP Transceivers

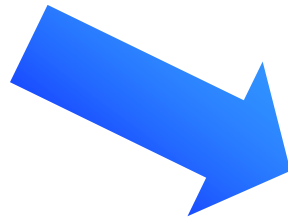
# Additional Setup Details

- Refer to ml505\_overview\_setup document for details on:
  - Software Requirements
  - ML505 Board Setup
    - **Equipment and Cables**
    - **Software**
    - **Network**
  - Terminal Programs
    - **This presentation requires the 9600-8-N-1 Baud terminal setup**



# ISE Software Requirement

- Xilinx ISE 10.1i SP3 software



# ChipScope Software Requirement

- Xilinx ChipScope Pro 10.1i SP3



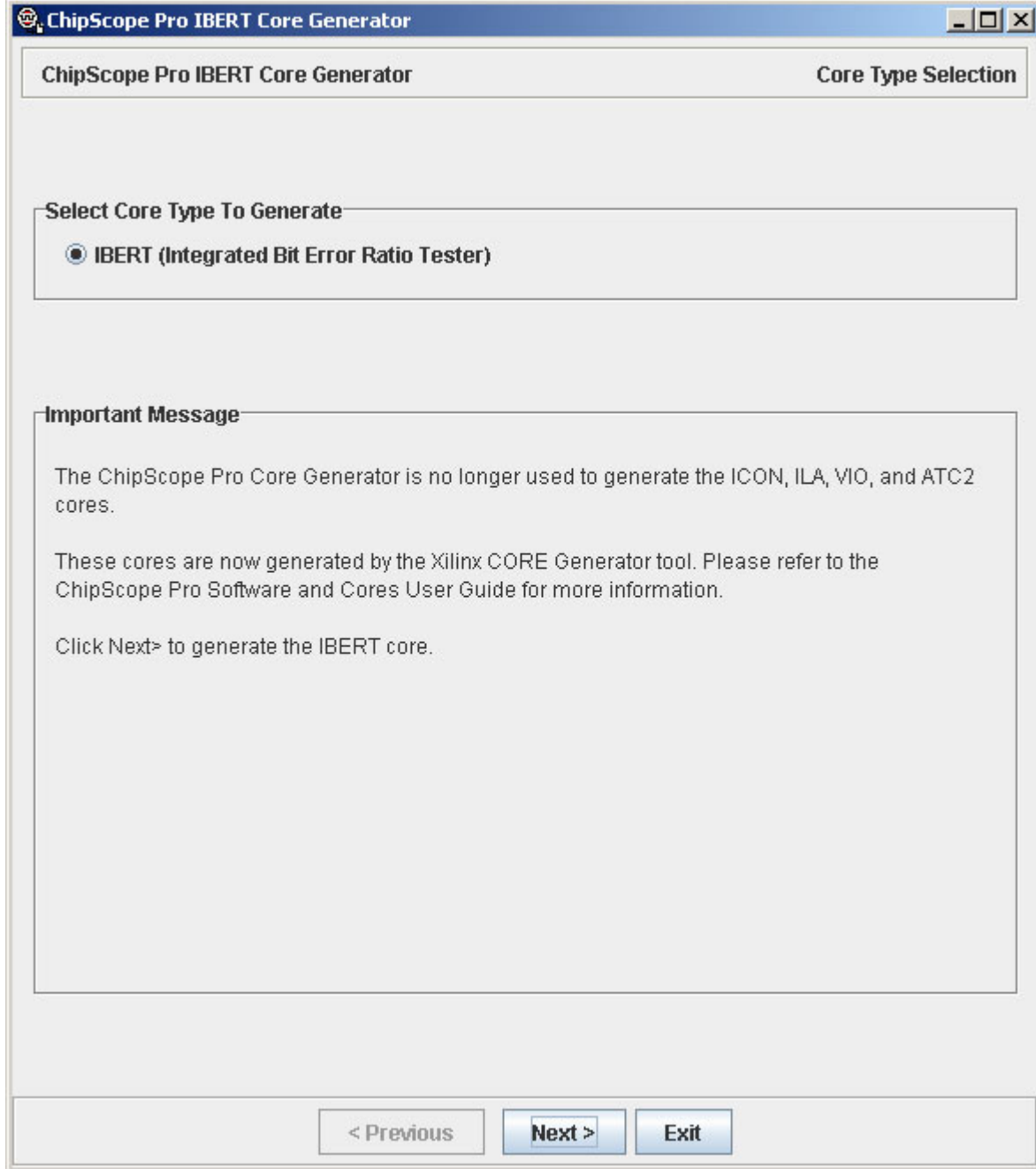
**ChipScope Pro Analyzer**

Release Version: 10.1 03  
Application Version: K.39 (Build 10103.8.234.834)  
Copyright (c) 1995-2008 Xilinx, Inc.  
All rights reserved.

# IBERT Generation

- Open the ChipScope Pro IBERT Core Generator



# IBERT Generation

- Set the output to your design directory
- Make these settings:
  - Virtex5
  - xc5vlx50t
  - ff1136
  - -1

ChipScope Pro IBERT Core Generator

IBERT General Options

Design Files

Output Bitstream: C:\ml505\_ibert\_4gtps\ml505\_ibert\_design.bit Browse

Device Selection

Device Family: Virtex5

Device: xc5vlx50t

Package: ff1136

Speed Grade: -1

Silicon Revision

Silicon Revision: Production

< Previous Next > Exit

# IBERT Generation

- System Clock Settings:
  - I/O Std: **LVC MOS33**
  - P Source Pin: **AH15**
  - Set Freq: **100**



The screenshot shows the 'ChipScope Pro IBERT Core Generator' window. The title bar includes the application name and standard window controls. The main window has a tab labeled 'IBERT' and a 'Clock Options' button in the top right corner. Below the tab is a section titled 'System Clock Settings' which contains three configuration fields: 'I/O Standard' is a dropdown menu set to 'LVC MOS33', 'P Source Pin' is a text input field containing 'AH15', and 'Frequency (MHz)' is a text input field containing '100'. At the bottom of the window, there are three buttons: '< Previous', 'Next >', and 'Exit'.

# IBERT Generation

- Set the Pattern Settings as shown

The screenshot shows the 'IBERT' configuration window in the 'MGT Options' section. The 'Resource Usage' section indicates that 0 out of 6 GTP Duals and 0 out of 12 DCMs are used. The 'Pattern Settings' section on the left contains a list of checkboxes, with the PRBS options (7-bit, 7-bit Alt, 9-bit, 11-bit, 15-bit, 20-bit, 23-bit, 29-bit, 31-bit) highlighted by a red box. The 'GTP Settings' section on the right is divided into two panels for GTP\_DUAL\_X0Y0 (MGT122) and GTP\_DUAL\_X0Y1 (MGT118). Each panel shows reference clock pins, TX and RX pin assignments for GTP 0 and GTP 1, and fields for Frequency Mode, Max Line Rate (Mbps), and Ref Clock Freq (MHz). At the bottom, there are navigation buttons for '< Previous', 'Next >', and 'Exit'.

IBERT MGT Options

Resource Usage  
Number of GTP Duals used: 0 out of 6 Number of DCMs used: 0 out of 12

Pattern Settings

- PRBS 7-bit
- PRBS 7-bit Alt
- PRBS 9-bit
- PRBS 11-bit
- PRBS 15-bit
- PRBS 20-bit
- PRBS 23-bit
- PRBS 29-bit
- PRBS 31-bit
- User Pattern
- Framed Counter
- Idle Pattern

GTP Settings

Enable GTP\_DUAL\_X0Y0 (MGT122)

Ref Clock Pins (P, N): AL5, AL4

|        | TX Pins (P, N) | RX Pins (P, N) |
|--------|----------------|----------------|
| GTP 0: | AK2, AL2       | AL1, AM1       |
| GTP 1: | AN4, AN3       | AP3, AP2       |

Frequency Mode: Invalid Line Rate

Max Line Rate (Mbps):

Ref Clock Freq (MHz):

Enable GTP\_DUAL\_X0Y1 (MGT118)

Ref Clock Pins (P, N): AF4, AF3

|        | TX Pins (P, N) | RX Pins (P, N) |
|--------|----------------|----------------|
| GTP 0: | AD2, AE2       | AE1, AF1       |
| GTP 1: | AJ2, AH2       | AH1, AG1       |

Frequency Mode: Invalid Line Rate

Max Line Rate (Mbps):

Ref Clock Freq (MHz):

< Previous Next > Exit

# IBERT Generation

- Select Enable GTP\_DUAL\_X0Y1
  - Set Max Line Rate to **2500**
  - Set Ref Clock Frequency to **100**
- Select Enable GTP\_DUAL\_X0Y2
  - Set Max Line Rate to **3000**
  - Set Ref Clock Frequency to **150**

ChipScope Pro IBERT Core Generator

IBERT MGT Options

Resource Usage

Number of GTP Duals used: 2 out of 6 Number of DCMs used: 6 out of 12

Pattern Settings

- PRBS 7-bit
- PRBS 7-bit Alt
- PRBS 9-bit
- PRBS 11-bit
- PRBS 15-bit
- PRBS 20-bit
- PRBS 23-bit
- PRBS 29-bit
- PRBS 31-bit
- User Pattern
- Framed Counter
- Idle Pattern

GTP Settings

Enable GTP\_DUAL\_X0Y1 (MGT118)

Ref Clock Pins (P, N): AF4, AF3

|        | TX Pins (P, N) | RX Pins (P, N) |
|--------|----------------|----------------|
| GTP 0: | AD2, AE2       | AE1, AF1       |
| GTP 1: | AJ2, AH2       | AH1, AG1       |

Frequency Mode: High Freq (1200Mbps - 3750Mbps)

Max Line Rate (Mbps): 2500

Ref Clock Freq (MHz): 100.00 (FB=5, REF=2, DIVSEL=1)

Enable GTP\_DUAL\_X0Y2 (MGT114)

Ref Clock Pins (P, N): Y4, Y3

|        | TX Pins (P, N) | RX Pins (P, N) |
|--------|----------------|----------------|
| GTP 0: | V2, W2         | W1, Y1         |
| GTP 1: | AC2, AB2       | AB1, AA1       |

Frequency Mode: High Freq (1200Mbps - 3750Mbps)

Max Line Rate (Mbps): 3000

Ref Clock Freq (MHz): 150.00 (FB=2, REF=1, DIVSEL=1)

< Previous Next > Exit

# IBERT Generation

- Select Enable GTP\_DUAL\_X0Y3
  - Set Max Line Rate to **2500**
  - Set Ref Clock Frequency to **125**
- Select Enable GTP\_DUAL\_X0Y4
  - Set Max Line Rate to **3000**
  - Set Ref Clock Frequency to **150**

The screenshot shows the 'IBERT' configuration window in the 'MGT Options' section. It is divided into 'Pattern Settings' and 'GTP Settings'.

**Pattern Settings:**

- PRBS 7-bit
- PRBS 7-bit Alt
- PRBS 9-bit
- PRBS 11-bit
- PRBS 15-bit
- PRBS 20-bit
- PRBS 23-bit
- PRBS 29-bit
- PRBS 31-bit
- User Pattern
- Framed Counter
- Idle Pattern

**Resource Usage:**

- Number of GTP Duals used: 4 out of 6
- Number of DCMs used: 12 out of 12

**GTP Settings (GTP\_DUAL\_X0Y3 - MGT112):**

- Enable GTP\_DUAL\_X0Y3 (MGT112)
- Ref Clock Pins (P, N): P4, P3

|        | TX Pins (P, N) | RX Pins (P, N) |
|--------|----------------|----------------|
| GTP 0: | M2, N2         | N1, P1         |
| GTP 1: | U2, T2         | T1, R1         |

- Frequency Mode: High Freq (1200Mbps - 3750Mbps)
- Max Line Rate (Mbps): 2500
- Ref Clock Freq (MHz): 125.00 (FB=2, REF=1, DIVSEL=1)

**GTP Settings (GTP\_DUAL\_X0Y4 - MGT116):**

- Enable GTP\_DUAL\_X0Y4 (MGT116)
- Ref Clock Pins (P, N): H4, H3

|        | TX Pins (P, N) | RX Pins (P, N) |
|--------|----------------|----------------|
| GTP 0: | F2, G2         | G1, H1         |
| GTP 1: | L2, K2         | K1, J1         |

- Frequency Mode: High Freq (1200Mbps - 3750Mbps)
- Max Line Rate (Mbps): 3000
- Ref Clock Freq (MHz): 150.00 (FB=2, REF=1, DIVSEL=1)

Navigation buttons: < Previous, Next >, Exit

# IBERT Generation

- Leave this screen as is



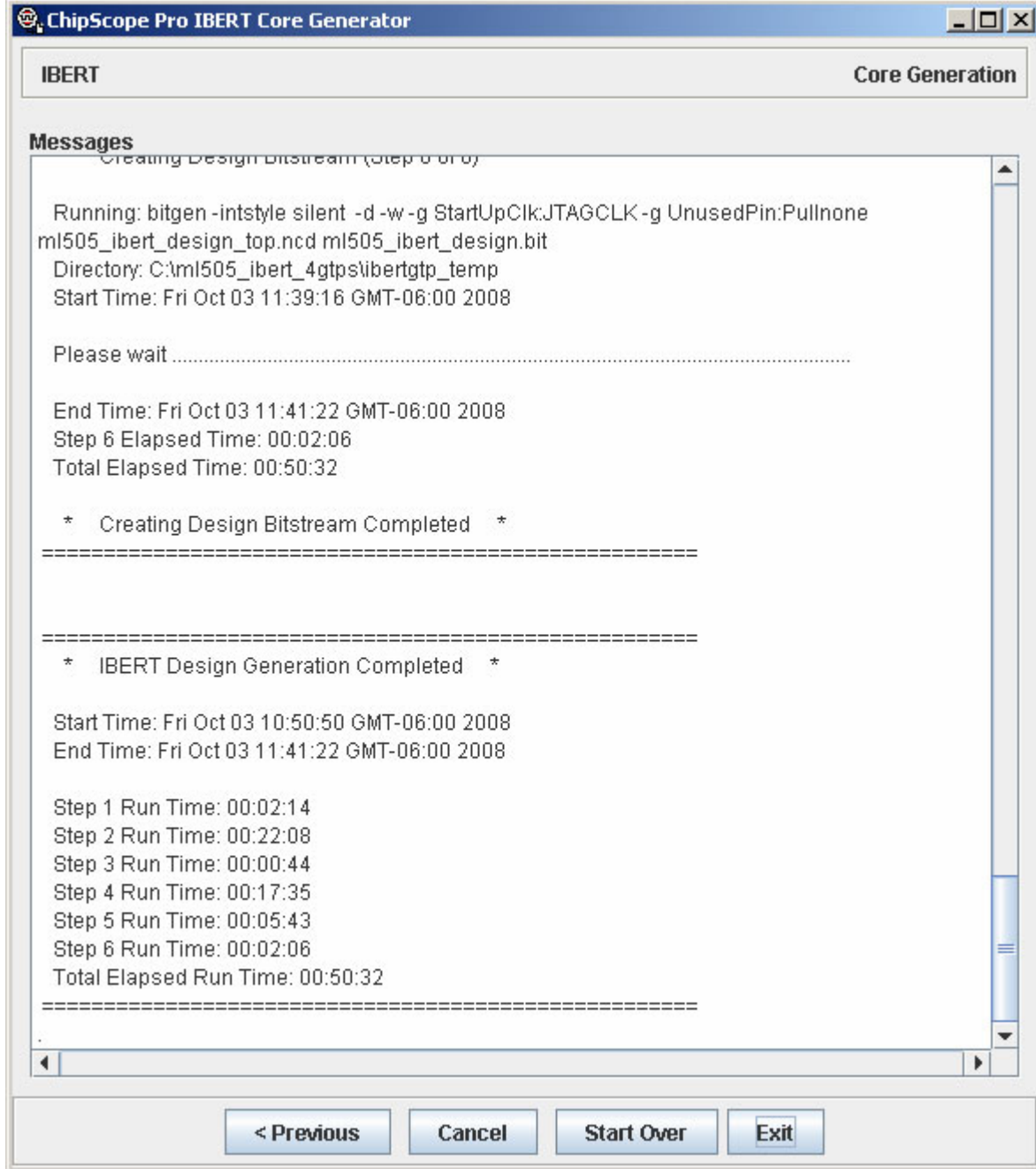
# IBERT Generation

- Click Generate Design



# IBERT Generation

- Bitstream is compiled and ready to use



# Documentation

- Virtex-5
  - Silicon Devices  
<http://www.xilinx.com/products/devices.htm>
  - Virtex-5 Multi-Platform FPGA  
<http://www.xilinx.com/products/virtex5/index.htm>
  - Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds100.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf)
  - Virtex-5 FPGA DC and Switching Characteristics Data Sheet  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds202.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf)

# Documentation

- Virtex-5
  - Virtex-5 FPGA User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug190.pdf](http://www.xilinx.com/support/documentation/user_guides/ug190.pdf)
  - Virtex-5 FPGA Configuration User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug191.pdf](http://www.xilinx.com/support/documentation/user_guides/ug191.pdf)
  - Virtex-5 System Monitor User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug192.pdf](http://www.xilinx.com/support/documentation/user_guides/ug192.pdf)
  - Virtex-5 Packaging and Pinout Specification  
[http://www.xilinx.com/support/documentation/user\\_guides/ug195.pdf](http://www.xilinx.com/support/documentation/user_guides/ug195.pdf)

# Documentation

- Virtex-5 RocketIO
  - RocketIO GTP Transceivers  
<http://www.xilinx.com/products/virtex5/lxt.htm>
  - RocketIO GTP Transceiver User Guide – UG196  
[http://www.xilinx.com/support/documentation/user\\_guides/ug196.pdf](http://www.xilinx.com/support/documentation/user_guides/ug196.pdf)
  - RocketIO GTX Transceivers  
<http://www.xilinx.com/products/virtex5/fxt.htm>
  - RocketIO GTX Transceiver User Guide – UG198  
[http://www.xilinx.com/support/documentation/user\\_guides/ug198.pdf](http://www.xilinx.com/support/documentation/user_guides/ug198.pdf)

# Documentation

- Design Resources

- ISE Development Tools and IP

<http://www.xilinx.com/ise>

- Integrated Software Environment (ISE) Foundation Resources

[http://www.xilinx.com/ise/logic\\_design\\_prod/foundation.htm](http://www.xilinx.com/ise/logic_design_prod/foundation.htm)

- ISE Manuals

[http://www.xilinx.com/support/software\\_manuals.htm](http://www.xilinx.com/support/software_manuals.htm)

- ISE Development System Reference Guide

<http://toolbox.xilinx.com/docsan/xilinx10/books/docs/dev/dev.pdf>

- ISE Development System Libraries Guide

[http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5\\_hdl/virtex5\\_hdl.pdf](http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5_hdl/virtex5_hdl.pdf)

# Documentation

- Additional Design Resources
  - Customer Support  
<http://www.xilinx.com/support>
  - Xilinx Design Services:  
<http://www.xilinx.com/xds>
  - Titanium Dedicated Engineering:  
<http://www.xilinx.com/titanium>
  - Education Services:  
<http://www.xilinx.com/education>
  - Xilinx On Board (Board and kit locator):  
<http://www.xilinx.com/xob>

# Documentation

- Platform Studio
  - Embedded Development Kit (EDK) Resources  
<http://www.xilinx.com/edk>
  - Embedded System Tools Reference Manual  
[http://www.xilinx.com/support/documentation/sw\\_manuals/edk10\\_est\\_rm.pdf](http://www.xilinx.com/support/documentation/sw_manuals/edk10_est_rm.pdf)
  - EDK Concepts, Tools, and Techniques  
[http://www.xilinx.com/support/documentation/sw\\_manuals/edk\\_ctt.pdf](http://www.xilinx.com/support/documentation/sw_manuals/edk_ctt.pdf)

# Documentation

- PowerPC 440
  - Embedded Processor Block in Virtex-5 FPGAs Reference Guide – UG200  
[http://www.xilinx.com/support/documentation/user\\_guides/ug200.pdf](http://www.xilinx.com/support/documentation/user_guides/ug200.pdf)
  - PPC440 Virtex-5 Wrapper – DS621  
[http://www.xilinx.com/support/documentation/ip\\_documentation/ppc440\\_virtex5.pdf](http://www.xilinx.com/support/documentation/ip_documentation/ppc440_virtex5.pdf)
  - DDR2 Memory Controller for PowerPC 440 Processors – DS567  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds567.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds567.pdf)

# Documentation

- MicroBlaze
  - MicroBlaze Processor  
<http://www.xilinx.com/microblaze>
  - MicroBlaze Processor Reference Guide – UG081  
[http://www.xilinx.com/support/documentation/sw\\_manuals/mb\\_ref\\_guide.pdf](http://www.xilinx.com/support/documentation/sw_manuals/mb_ref_guide.pdf)

# Documentation

- ChipScope Pro
  - ChipScope Pro 10.1i Serial IO Toolkit User Manual  
[http://www.xilinx.com/ise/verification/chipscope\\_pro\\_siotk\\_10\\_1\\_ug213.pdf](http://www.xilinx.com/ise/verification/chipscope_pro_siotk_10_1_ug213.pdf)
  - ChipScope Pro 10.1i ChipScope Pro Software and Cores User Guide  
[http://www.xilinx.com/ise/verification/chipscope\\_pro\\_sw\\_cores\\_10\\_1\\_ug029.pdf](http://www.xilinx.com/ise/verification/chipscope_pro_sw_cores_10_1_ug029.pdf)

# Documentation

- Memory Solutions

- Demos on Demand – Memory Interface Solutions with Xilinx FPGAs

[http://www.demosondemand.com/clients/xilinx/001/page\\_new2/index.asp#35](http://www.demosondemand.com/clients/xilinx/001/page_new2/index.asp#35)

- Xilinx Memory Corner

[http://www.xilinx.com/products/design\\_resources/mem\\_corner](http://www.xilinx.com/products/design_resources/mem_corner)

- Additional Memory Resources

<http://www.xilinx.com/support/software/memory/protected/index.htm>

- Xilinx Memory Interface Generator (MIG) 2.1 User Guide

<http://www.xilinx.com/support/software/memory/protected/ug086.pdf>

- Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator

[http://www.xilinx.com/support/documentation/white\\_papers/wp260.pdf](http://www.xilinx.com/support/documentation/white_papers/wp260.pdf)

# Documentation

- Ethernet
  - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet  
[http://www.xilinx.com/support/documentation/ip\\_documentation/v5\\_emac\\_ds550.pdf](http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_ds550.pdf)
  - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide  
[http://www.xilinx.com/support/documentation/ip\\_documentation/v5\\_emac\\_gsg340.pdf](http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_gsg340.pdf)
  - Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug194.pdf](http://www.xilinx.com/support/documentation/user_guides/ug194.pdf)
  - LightWeight IP (lwIP) Application Examples – XAPP1026  
[http://www.xilinx.com/support/documentation/application\\_notes/xapp1026.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp1026.pdf)

# Documentation

- PCIe
  - LogiCORE Endpoint Block Plus for PCI Express Data Sheet  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_ds551.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ds551.pdf)
  - LogiCORE Endpoint Block Plus for PCI Express Designs  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_ug341.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ug341.pdf)
  - LogiCORE Endpoint Block Plus Getting Started Guide for PCI Express Designs  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_gsg343.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_gsg343.pdf)
  - Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs  
[http://www.xilinx.com/support/documentation/user\\_guides/ug197.pdf](http://www.xilinx.com/support/documentation/user_guides/ug197.pdf)

# Documentation

- System Generator
  - System Generator for DSP  
<http://www.xilinx.com/sysgen>
  - Xilinx System Generator for DSP User Guides  
[http://www.xilinx.com/support/documentation/sw\\_manuals/sysgen\\_bklist.pdf](http://www.xilinx.com/support/documentation/sw_manuals/sysgen_bklist.pdf)
  - XtremeDSP Design Considerations  
[http://www.xilinx.com/support/documentation/user\\_guides/ug193.pdf](http://www.xilinx.com/support/documentation/user_guides/ug193.pdf)

# Documentation

- PLB v4.6 IP
  - Processor Local Bus (PLB) v4.6 Data Sheet – DS531  
[http://www.xilinx.com/support/documentation/ip\\_documentation/plb\\_v46.pdf](http://www.xilinx.com/support/documentation/ip_documentation/plb_v46.pdf)
  - Multi-Port Memory Controller (MPMC) – DS643  
[http://www.xilinx.com/support/documentation/ip\\_documentation/mpmc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/mpmc.pdf)
  - XPS Multi-Channel External Memory Controller (XPS MCH EMC) – DS575  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_mch\\_emc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_mch_emc.pdf)
  - XPS LocalLink TEMAC – DS537  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_ll\\_temac.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_temac.pdf)
  - XPS LocalLink FIFO – DS568  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_ll\\_fifo.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_fifo.pdf)

# Documentation

- PLB v4.6 IP
  - XPS IIC Bus Interface – DS606  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_iic.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_iic.pdf)
  - XPS SYSACE (System ACE) Interface Controller – DS583  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_sysace.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_sysace.pdf)
  - XPS Timer/Counter – DS573  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_timer.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_timer.pdf)
  - XPS Interrupt Controller – DS572  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_intc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_intc.pdf)
  - Using and Creating Interrupt-Based Systems Application Note  
[http://www.xilinx.com/support/documentation/application\\_notes/xapp778.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp778.pdf)

# Documentation

- PLB v4.6 IP
  - XPS General Purpose Input/Output (GPIO) – DS569  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_gpio.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_gpio.pdf)
  - XPS External Peripheral Controller (EPC) – DS581  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_epc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_epc.pdf)
  - XPS 16550 UART – DS577  
[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_uart16550.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_uart16550.pdf)
  - PLBV46 to DCR Bridge Data Sheet – DS578  
[http://www.xilinx.com/support/documentation/ip\\_documentation/plbv46\\_dcr\\_bridge.pdf](http://www.xilinx.com/support/documentation/ip_documentation/plbv46_dcr_bridge.pdf)

# Documentation

- IP
  - Local Memory Bus Data Sheet – DS445  
[http://www.xilinx.com/support/documentation/ip\\_documentation/lmb\\_v10.pdf](http://www.xilinx.com/support/documentation/ip_documentation/lmb_v10.pdf)
  - Block RAM Block Data Sheet – DS444  
[http://www.xilinx.com/support/documentation/ip\\_documentation/bram\\_block.pdf](http://www.xilinx.com/support/documentation/ip_documentation/bram_block.pdf)
  - Microprocessor Debug Module Data Sheet – DS641  
[http://www.xilinx.com/support/documentation/ip\\_documentation/mdm.pdf](http://www.xilinx.com/support/documentation/ip_documentation/mdm.pdf)
  - LMB Block RAM Interface Controller Data Sheet – DS452  
[http://www.xilinx.com/support/documentation/ip\\_documentation/lmb\\_bram\\_if\\_cntlr.pdf](http://www.xilinx.com/support/documentation/ip_documentation/lmb_bram_if_cntlr.pdf)
  - Device Control Register Bus (DCR) v2.9 Data Sheet – DS406  
[http://www.xilinx.com/support/documentation/ip\\_documentation/dcr\\_v29.pdf](http://www.xilinx.com/support/documentation/ip_documentation/dcr_v29.pdf)

# Documentation

- IP
  - JTAGPPC Controller Data Sheet – DS298  
[http://www.xilinx.com/support/documentation/ip\\_documentation/jtagppc\\_cntlr.pdf](http://www.xilinx.com/support/documentation/ip_documentation/jtagppc_cntlr.pdf)
  - Processor System Reset Module Data Sheet – DS402  
[http://www.xilinx.com/support/documentation/ip\\_documentation/proc\\_sys\\_reset.pdf](http://www.xilinx.com/support/documentation/ip_documentation/proc_sys_reset.pdf)
  - Clock Generator v2.0 Data Sheet – DS614  
[http://www.xilinx.com/support/documentation/ip\\_documentation/clock\\_generator.pdf](http://www.xilinx.com/support/documentation/ip_documentation/clock_generator.pdf)
  - Util Bus Split Operation Data Sheet – DS484  
[http://www.xilinx.com/support/documentation/ip\\_documentation/util\\_bus\\_split.pdf](http://www.xilinx.com/support/documentation/ip_documentation/util_bus_split.pdf)

# Documentation

- ML505/506/507
  - ML505 Overview  
<http://www.xilinx.com/ml505>
  - ML506 Overview  
<http://www.xilinx.com/ml506>
  - ML507 Overview  
<http://www.xilinx.com/ml507>
  - ML505/506/507 Evaluation Platform User Guide – UG347  
[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug347.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug347.pdf)
  - ML505/506/507 Getting Started Tutorial – UG348  
[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug348.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug348.pdf)
  - ML505/506/507 Reference Design User Guide – UG349  
[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug349.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug349.pdf)

# Documentation

- ML505/506/507
  - ML505/506/507 Schematics  
[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ml50x\\_schematics.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ml50x_schematics.pdf)
  - ML505/506/507 Bill of Material  
[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ml505\\_501\\_bom.xls](http://www.xilinx.com/support/documentation/boards_and_kits/ml505_501_bom.xls)