



ML505 GTP Aurora Design with CRC Addition - Simulation and Synthesis

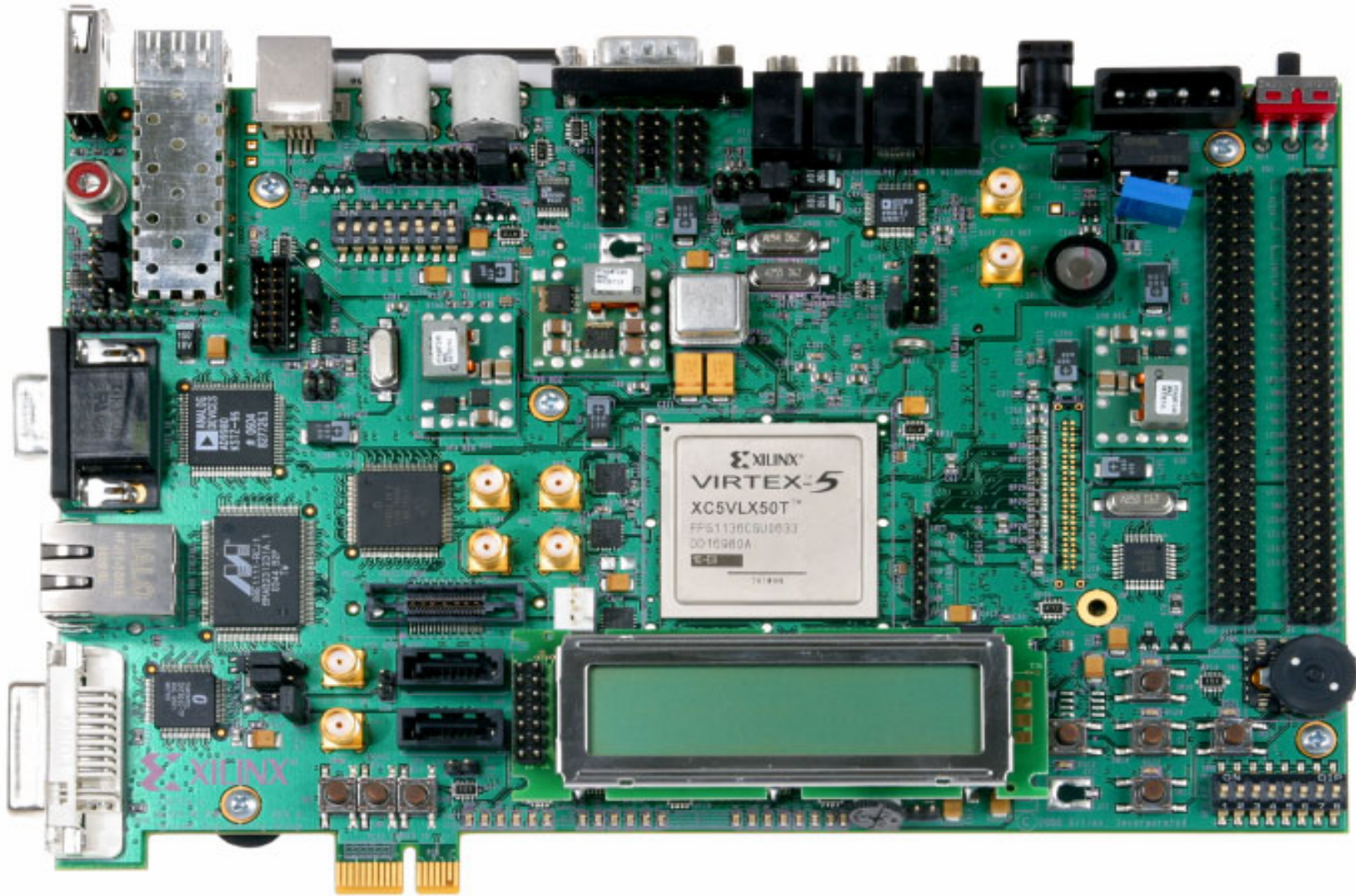
June 2007

GTP Aurora Overview

- The GTP Aurora with CRC addition reference design demonstrates the usage of a 2 byte, single lane aurora design interfaced with CRC32. The reference design is interfaced with GTP transceiver.
- This reference design can be demonstrated on a ML505 board. This demo comprises of :
 - Hardware Setup
 - Design - Simulation and Synthesis
 - Testing the Design



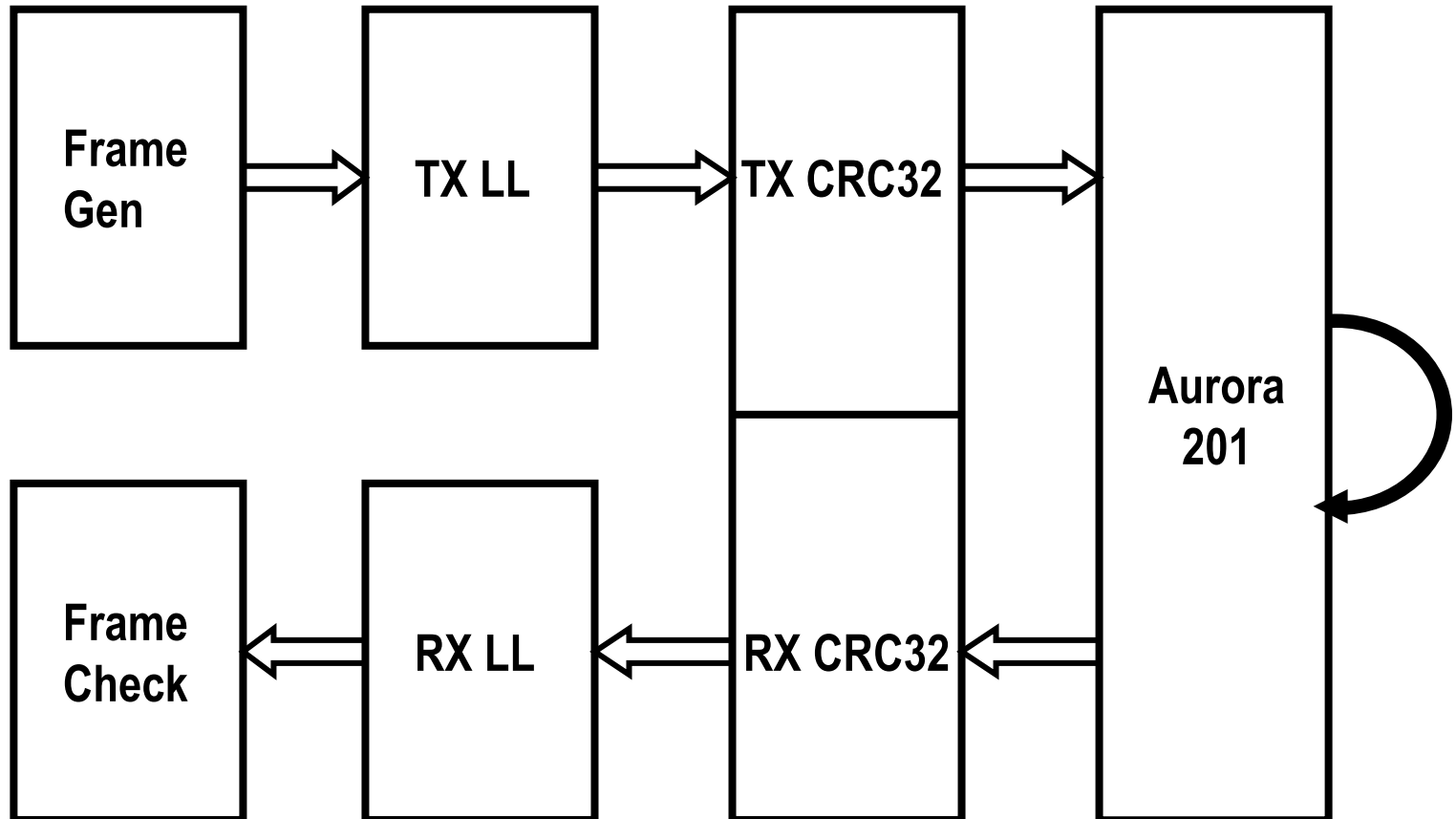
Xilinx ML505 Board



Design Configuration

- Aurora 201 :
 - 16 bit Protocol Data Unit interface
 - Single lane
 - Consists of User flow control and Native flow control interfaces
 - UCF modified to suit ML505 boards
 - Target device is Virtex-5 XC5VLX50T
 - Line rate is 3.125 Gbps & Reference Clock is 156.25 MHz
- CRC32 :
 - 32 bit data input & 32 bit CRC output
 - Built around CRC32 hard macro available in Virtex-5 XC5VLX50T

Block diagram of Aurora CRC Interface



Aurora 201 - CRC - Example design

- The pre-built design is available in Verilog
- Unzip the ml505_vlog_crc_aurora_201.zip file to your project directory
- These files have been prepared for your convenience and it will add several required files and a pre-built design with a bitstream



Simulating the Example Design

- The design includes several scripts to assist the user in running the Xilinx ISE software.
- The GTP Aurora core provides a command line script to simulate the example design. To run the Verilog ModelSim simulation of the Aurora core, use the following instructions:
 1. For simulating the Verilog design, launch the ModelSim simulator and set the current directory to:
`<project directory>/ml505_vlog_crc_aurora_201`
 2. Set the MTI_LIBS variable:
`modelsim> setenv MTI_LIBS <path to compiled libraries>`
 3. Launch the simulation script:
`modelsim> do crc_aurora.do`



Simulating the Example Design

- The GTP Aurora core provides a quick way to simulate and observe the behavior of the core using the provided example design.
- Prior to simulating the core, the functional (gate-level) simulation models must be generated.
- You must compile all source files in the following directories to a single library as shown in table below:
 - Verilog → Library → `<Xilinx dir>/verilog/src/unisims`
`<Xilinx dir>/smartmodel/<OS>/wrappers/mtiverilog`



Simulating the Example Design

- The ModelSim script compiles the example design and testbench, and adds the relevant signals to the wave window.
- After the design is compiled and the wave window is displayed, run the simulation for about 20 μ s.
- The design is reset, followed by Aurora channel initialization and data transfer.
- Data transfer begins after the CHANNEL_UP signal goes high.
- On the TX side CRC is calculated and appended after every data frame with EOF_N.
- On the RX side, CRC is calculated only for the RX data. The re-calculated CRC is compared against the CRC value received through the link



Implementing the Verilog Design

- The design includes several scripts to assist the user in running the Xilinx ISE software.
- From the command prompt, navigate to the project directory and type the following:
 - For Windows:

```
ms-dos> cd ml505_vlog_crc_aurora_201
ms-dos> xilperl make_aurora.pl -m -p -b -example
```
 - For UNIX:

```
unix-shell% cd ml505_vlog_crc_aurora_201
unix-shell% xilperl make_aurora.pl -m -p -b -example
```
- These commands execute a script that synthesizes, builds, maps, place-and-routes the example design and produces a bitmap file. The resulting files are placed in the scripts directory.



Example Design Hierarchy

```
example_tb
|__aurora_example
|   |__aurora_201
|   |   |__aurora_lane
|   |   |   |__lane_init_sm
|   |   |   |__chbond_count_dec
|   |   |   |__sym_gen
|   |   |   |__sym_dec
|   |   |   |__error_detect
|   |   |__phase_align
|   |   |__global_logic
|   |   |   |__channel_init_sm
|   |   |   |__idle_and_ver_gen
|   |   |   |__channel_error_detect
|   |   |__tx_ll
|   |   |   |__tx_ll_datapath
|   |   |   |__tx_ll_control
|   |   |__rx_ll
|   |   |   |__rx_ll_nfc
|   |   |   |__ufc_filter
|   |   |   |__rx_ll_pdu_datapath
|   |   |   |__rx_ll_ufc_datapath
|   |   |__v5tx_crc
|   |   |__v5rx_crc
|   |__standard_cc_module
|   |__frame_gen
|   |__frame_check
```



Documentation

- GTP Aurora
 - LogiCORE GTP Aurora Getting Started Guide
http://www.xilinx.com/aurora/aurora_member/aurora_gs_ug223.pdf
 - LogiCORE GTP Aurora User Guide
http://www.xilinx.com/aurora/aurora_member/ug224.pdf
 - LogiCORE GTP Aurora Data Sheet
<http://www.xilinx.com/aurora/aurorads538.pdf>
- CRC
 - LogiCORE CRC Wizard Datasheet
http://www.xilinx.com/bvdocs/ipcenter/data_sheet/crc_wiz_ds589.pdf
 - LogiCORE CRC Wizard User Guide
http://www.xilinx.com/bvdocs/ipcenter/data_sheet/crc_wiz_ug189.pdf



Documentation

- ML505
 - ML505 Overview
<http://www.xilinx.com/ml505>
 - ML505 User Guide – UG347
<http://www.xilinx.com/bvdocs/userguides/ug347.pdf>
 - ML505 Getting Started Tutorial – UG348
<http://www.xilinx.com/bvdocs/userguides/ug348.pdf>
 - ML505 Schematics
http://www.xilinx.com/products/boards/ml505/docs/ml505_20061205_bw.pdf

