ML50x System Monitor Demonstration

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Overview

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• System Monitor Overview
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Goals

• Demonstrate the ability of the System Monitor feature built into all Virtex-5 devices

• Show a closed loop system that regulates temperature using System Monitor

• Use standard supported IP
  – Demonstrations use the EDK xps_sysmon_adc peripheral
System Monitor Overview

- Built into every Virtex-5 device
- 10-bit, 200 kSPS (kilosamples per second) Analog-to-Digital Converter (ADC)
- Monitors up to 17 external channels
- Internal sensors for temperature, Vccint and Vccaux
- Always on, active even before configuration

- Can protect FPGA from over-temperature condition
- Full JTAG and fabric access.
- Can monitor board level sensors with external channels
- Channel sequencing, data filtering, and alarms / interrupts for autonomous operation
- Fully supported EDK peripheral

Note: Presentation applies to all ML50x boards
Xilinx ML505 Board

- ML505 shown; the ML506 uses an XC5VSX50T; the ML507 uses an XC5VFX70T
Hardware Setup

- Connect the Xilinx Platform USB / Parallel Cable IV (PC4) to the ML505 board

- Connect the RS232 null modem cable to the ML505 board
Optional Hardware Setup

Two of the three demos make use of a user supplied fan mounted on the FPGA

- A suitable fan for the ML505 (or any Xilinx FPGA board) can be obtained from Radian Heat Sinks: [http://www.radianheatsinks.com/virtex-chart.pdf](http://www.radianheatsinks.com/virtex-chart.pdf)
- The particular model used for the ML505 is (5V) FB35-K52B-T710

Note: Presentation applies to all ML50x boards
Additional Setup Details

• Refer to ml505_overview_setup.ppt for details on:
  – Software Requirements
  – ML505 Board Setup
    • Equipment and Cables
    • Software
    • Network
  – Terminal Programs
    • This presentation requires the 9600-8-N-1 Baud terminal setup*

*115200-8-N-1 Baud is used for Demo 1

Note: Presentation applies to all ML50x boards
ISE Software Requirement

• Xilinx ISE 10.1 SP2 software

Note: Presentation applies to all ML50x boards
EDK Software Requirement

- Xilinx EDK 10.1 SP2 software
Software Setup

• Start the Terminal Program:
  – HyperTerminal is recommended
  – Settings files included in the etc/*.ht directory
Optional Software

- ChipScope™ Pro 10.1 Analyzer
  - While not required, the ChipScope Pro Analyzer is a great way to visualize the FPGA temperature and voltages in real time.
  - The System Monitor is supported in ChipScope 9.1i and later

Open the JTAG cable, and double click on ‘System Monitor Console’
Using The Demos
Using the Demos

Three demonstrations are provided:

1. **Demo1**: Live monitoring of temperature, voltage, current and power*, using the SysMon EDK peripheral.
2. **Demo2**: A demonstration of ‘basic’ fan control using the SysMon.
   - Holds the FPGA system between an upper and lower temperature
3. **Demo3**: A demonstration of accurate fan speed regulation using the SysMon.
   - Holds the FPGA exactly at a given temperature (within 0.1C)

Note: A custom IP pcore, known as the heater pcore* is also used. The heater pcore is not a supported product. Please see disclaimer on slide 15.

*Current and hence power can be monitored on boards, such as the ML550, that have a shunt resistor. The ML50x platforms are set up to monitor voltage and temperature only.

Note: Presentation applies to all ML50x boards
Heater Core Disclaimer

- The ‘Heater Core’ used in this design is for demonstration purposes only
  - It is not intended for general purpose use
  - It is not supported by Xilinx
  - It is not intended to draw an accurate amount of current
  - Its only function is to draw enough current to heat the device for demonstrations
  - Care should be taken when using the heater core, as the FPGA temperature/current can increase dramatically. Never exceed the rated FPGA limits
Locating the Pre-Built Designs

- Unzip `ml505_std_ip_sysmon.zip` and locate the pre-built ACE files, or the bitstreams:
  - `ml505_std_ip_sysmon/ace/ml505_SysMon*.ace`
  - `ml505_std_ip_sysmon/implementation/ml505_SysMon*.bit`
Using the Demos

Run the demonstration using one of the two following options:

1. Copy the provided ACE file onto a CompactFlash card to configure the ML50x: (See slide 30 for instructions)
   - ace/ml505_SYSMon_Demo.ace
   - ace/ml505_SYSMon_Fan_Control.ace
   - ace/ml505_SYSMon_Fan_Regulate.ace

2. Download the pre-built bitstreams using ISE iMPACT:
   - implementation/ml505_SYSMon_Demo.bit
   - implementation/ml505_SYSMon_Fan_Control.bit
   - Implementation/ml505_SYSMon_Fan_Regulate.bit
Using Demo 1

Live monitoring of temperature, voltage, current and power*

- This demo reads the SysMon sensors and displays them on the terminal.
- A heater core can also be activated in order to increase the temperature, and the effect can be seen immediately on the display.
- See the next slides for instructions and sample output

*Current and hence power can be monitored on boards, such as the ML550, that have a shunt resistor. The ML50x platforms are set up to monitor voltage and temperature only.
Using Demo 1

- Download the `SysMon_Demo` demo using one of the previously described methods on slide 17.
- **Start HyperTerminal**
  - Note this demo uses the 115200-8-N-1 Baud terminal setup
  - The file `etc/115200.ht` can be used to automatically set this (COM1)
- **Start the ChipScope Pro tool (Optional)**
  - This gives a real time visual response of the FPGA voltage and temperature.
  - Open the JTAG Cable in the ChipScope Pro tool.
  - Double click on the ‘System Monitor Console’ to bring up the real-time graphs of voltage and temperature.

*Disclaimer: Care should be taken when using the heater core, as the FPGA temperature/current can increase dramatically. Never exceed rated FPGA limits*
Using Demo 1

Interactive Demo Options:

– The demo has a number of options which can be accessed from the terminal.
– Press any key to be presented with a menu, then pressing:
  – 1) Set the number of heater cores to make active (0-4)*
  – 2) Auto-Cycle the heater cores. This will turn on the heater cores one by one, and then off, repeating this loop.
  – 3) Reset the SysMon Min/Max values (useful for ChipScope)

* Disclaimer: Care should be taken when using the heater core, as the FPGA temperature/current can increase dramatically. Never exceed rated FPGA limits

Note: Presentation applies to all ML50x boards
Example Output

Demo 1

- IR drop on the board increases with the number of heaters. Max current draw ~10A

- ChipScope Output: FPGA temperature can be seen changing as the heater cores are turned on

- Terminal Output: SysMon Readings can be seen in real time. Current/Power would also be shown on an ML550

Note: Presentation applies to all ML50x boards
Using Demo 2

A demonstration of ‘basic’ fan control using the SysMon

- This demo reads the SysMon temperature and uses this to control a fan
- When the temperature hits a user-defined upper or lower limit*, the fan turns on or off
- A heater core can also be activated in order to increase the temperature, and the effect can be seen immediately on the display
- This example uses polling, but an interrupt based version is also possible
- See the next slides for instructions and sample output

* These limits can be adjusted by using the buttons on the board
Using Demo 2

- Ensure the fan is connected to the ML50x board
- Download the **SysMon_Fan_Control** demo using one of the previously described methods on slide 17
- Start HyperTerminal
  - Note this demo uses the 9600-8-N-1 Baud terminal setup
  - The file `etc/9600.ht` can be used to automatically set this (COM1)
- Start the ChipScope Pro tool (Optional)
  - This gives a real time visual response of the FPGA voltage and temperature.
  - Open the JTAG Cable in the ChipScope Pro tool.
  - Double click on the ‘System Monitor Console’ to bring up the real-time graphs of voltage and temperature.

*Disclaimer: Care should be taken when using the heater core, as the FPGA temperature/current can increase dramatically. Never exceed rated FPGA limits*
Using Demo 2

Interactive Demo Options:

– The demo has a number of options which are controlled by the board pushbuttons.
– The up/down arrows control the upper temperature limit (fan turn on limit)
– The left button enables the fan control
– The right button turns on all the heater cores*

* Disclaimer: Care should be taken when using the heater core, as the FPGA temperature/current can increase dramatically. Never exceed rated FPGA limits
Example Output

ChipScope Output
FPGA temperature can be seen changing between upper and lower limits as the fan is turned off and on.

Terminal Output
SysMon Readings can be seen in real time.

Note: Presentation applies to all ML50x boards
Using Demo 3

A demonstration of accurate fan speed regulation using the SysMon

• This demo uses the SysMon temperature, and implements a PI* control algorithm to adjust the fan speed.
• Can control FPGA temperature with an accuracy of 0.1C
• The performance of the SysMon driven fan controller is better than the dedicated IC on the ML50x – from the dedicated IC datasheet, measurement errors of 25C are possible.
• This solution allows customers to remove the fan controller IC from a PCB, for cost savings and increased performance
• See the next slides for instructions and sample output

* PI refers to Proportional-Integral Control.

Note: Presentation applies to all ML50x boards
Using Demo 3

- Ensure the fan is connected to the ML50x board
- Download the **SysMon_Fan_Regulate** demo using one of the previously described methods on slide 17.

- **Start HyperTerminal**
  - Note this demo uses the 9600-8-N-1 Baud terminal setup
  - The file **etc/9600.ht** can be used to automatically set this (COM1)

- **Start the ChipScope Pro tool (Optional)**
  - This gives a real time visual response of the FPGA voltage and temperature.
  - Open the JTAG Cable in the ChipScope Pro tool.
  - Double click on the ‘System Monitor Console’ to bring up the real-time graphs of voltage and temperature.

*Disclaimer: Care should be taken when using the heater core, as the FPGA temperature/current can increase dramatically. Never exceed rated FPGA limits*
Using Demo 3

Interactive Demo Options:

- The demo has a number of options which are controlled by the board pushbuttons.
- The up/down arrows control the required temperature
- The left button enables the fan control
- The right button turns on all the heater cores*

* Disclaimer: Care should be taken when using the heater core, as the FPGA temperature/current can increase dramatically. Never exceed rated FPGA limits

Note: Presentation applies to all ML50x boards
Example Output

ChipScope Output
FPGA temperature can be seen to be regulated
Target was 65°C, then changed to 60°C

Terminal Output
SysMon Readings can be seen in real time. Also shows the fan speed, and the error < 0.1°C
Run ACE File

- Copy one of the .ace files to the ML50X\cfg6 directory on your CompactFlash card
  - **Important**: Delete any existing ace files in this cfg6 directory
  - **Note**: Use a CompactFlash reader to mount the CompactFlash as a disk drive
Run ACE File

- Eject the CompactFlash from your PC and insert it back into the ML505
- Type 6 to run the newly created ACE file
Demo BitGen Options

- Due to the presence of the heater core and its ability to draw a large amount of current, the Over-Temperature-Power-Down option should be enabled.
- Over-Temperature-Power-Down is a System Monitor feature that will shut down the FPGA if the temperature exceeds 125°C.
- Specify the bitgen –g option ‘OverTempPowerDown’ to enable over-temperature protection.
- The SysMon ‘Over Temperature’ alarm must also be enabled (this is taken care of in the software application, but is on by default).
- All the Demo bitstreams and ACE files have this enabled.
Documentation

• Virtex-5
  – System Monitor
    http://www.xilinx.com/systemmonitor
  – Silicon Devices
    http://www.xilinx.com/products/silicon_solutions
  – Virtex-5 Multi-Platform FPGA
  – Virtex-5 Family Overview: LX, LXT, and SXT Platforms
    http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
  – Virtex-5 FPGA Configuration User Guide
  – Virtex-5 FPGA DC and Switching Characteristics Data Sheet

Note: Presentation applies to all ML50x boards