ML505/506 Three GTPs IBERT QuickStart
Using 9.1i SP3 ChipScope™ Pro

April 2007
ML505 IBERT Overview

• Software Requirements
• Hardware Setup
  – SMA Loopback (Available at www.flrst.com)
  – Catalyst PCIe Tester (Available at www.getcatalyst.com)
• ChipScope Setup
• Running IBERT
  – Highlighting the Virtex-5 RocketIO™ GTP Transceivers
Additional Setup Details

• Refer to ml505_overview_setup document for details on:
  – Software Requirements
  – ML505 Board Setup
    • Equipment and Cables
    • Software
    • Network
  – Terminal Programs
    • This presentation requires the 9600-8-N-1 Baud terminal setup

Note: This presentation can be used for ML505 or ML506; see notes at bottom of these pages
ChipScope Software Requirement

- Xilinx ChipScope 9.1i SP3

Note: Presentation applies to the ML505 and ML506
Xilinx ML505 Board

Note: ML505 shown; the ML506 uses an XC5VSX50T FPGA
Setting Up the Hardware

• Connect the Xilinx Parallel Cable IV (PC4)
  – HW-PC4

• Optional - Pancake Fan
  – Recommended for keeping the Virtex-5 device cool
Setting Up the Hardware

- Set SW6 to 150 MHz frequency
  - For MGT116 (X0Y4)
  - Set SW6 (on back of board) to 11001010
  - See the ML505/506 User’s Guide, page 38 for more details

Table 1-30: Configurations for Clock Source and Frequency Options

<table>
<thead>
<tr>
<th>DIP Switch SW6 [1:8] Value</th>
<th>Input Ref Clock (MHz)</th>
<th>M Divider Value</th>
<th>N Divider Value</th>
<th>VCO (MHz)</th>
<th>Output Frequency (MHz)</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1 0 0 0 1 0 1</td>
<td>19.44</td>
<td>32</td>
<td>4</td>
<td>622.08</td>
<td>155.52</td>
<td>SONET</td>
</tr>
<tr>
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<td>19.44</td>
<td>32</td>
<td>8</td>
<td>622.08</td>
<td>77.76</td>
<td>SONET</td>
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<tr>
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<td>32</td>
<td>1</td>
<td>622.08</td>
<td>622.08</td>
<td>SONET</td>
</tr>
<tr>
<td>1 0 0 0 0 1 0 1</td>
<td>19.44</td>
<td>32</td>
<td>2</td>
<td>622.08</td>
<td>311.04</td>
<td>SONET</td>
</tr>
<tr>
<td>0 0 1 1 1 1 0 1</td>
<td>25</td>
<td>25</td>
<td>5</td>
<td>625</td>
<td>125</td>
<td>Gigabit Ethernet</td>
</tr>
<tr>
<td>1 1 1 1 1 0 1 0</td>
<td>25</td>
<td>25</td>
<td>10</td>
<td>625</td>
<td>62.5</td>
<td>Gigabit Ethernet</td>
</tr>
<tr>
<td>1 0 1 0 1 0 1 0</td>
<td>25</td>
<td>24</td>
<td>6</td>
<td>600</td>
<td>100</td>
<td>PCI Express</td>
</tr>
<tr>
<td>1 1 0 0 1 0 1 0</td>
<td>25</td>
<td>24</td>
<td>4</td>
<td>600</td>
<td>150(1)</td>
<td>SATA</td>
</tr>
<tr>
<td>0 1 1 0 0 1 0 1</td>
<td>25</td>
<td>24</td>
<td>8</td>
<td>600</td>
<td>75</td>
<td>SATA</td>
</tr>
<tr>
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<td>6</td>
<td>637.5</td>
<td>106.25</td>
<td>Fibre Channel</td>
</tr>
<tr>
<td>0 1 0 0 1 0 0 0</td>
<td>26.5625</td>
<td>24</td>
<td>3</td>
<td>637.5</td>
<td>212.5</td>
<td>Fibre Channel</td>
</tr>
<tr>
<td>1 1 0 0 1 0 0 0</td>
<td>26.5625</td>
<td>24</td>
<td>4</td>
<td>637.5</td>
<td>159.375</td>
<td>Fibre Channel</td>
</tr>
</tbody>
</table>

Note: Presentation applies to the ML505 and ML506
Setting Up the Hardware

• SMA Cable
  – www.flrst.com
  – P/N: ASPI-024-ASPI-S402
Setting Up the Hardware

• Using the SMA cables:
  – Connect J42 and J44
  – Connect J43 and J45

Note: Presentation applies to the ML505 and ML506
Setting Up the Hardware

- Connect Optical Loopback Adapter
  - [www.molex.com](http://www.molex.com)
  - SFP Loopback Adapter, 3.5 db Attenuation
  - Part # [74720-0501](http://www.molex.com)
  - Alternatively, use an SFP transceiver with a fiber optic cable
  - Insert into the SFP Connector on the ML505 board

Note: Presentation applies to the ML505 and ML506
Setting Up the Hardware

- PCIe Testing Hardware:
  - Catalyst PXP-100 DVT Platform
  - Catalyst PELOOP-BACK

Note: Presentation applies to the ML505 and ML506
Setting Up the Hardware

- On the Catalyst, set the reference clock jumper to open

- Insert the PELOOP-BACK into one of the PCIe slots

Note: Presentation applies to the ML505 and ML506
Setting Up the Hardware

- Insert the ML505 into the other slot
- Connect ML505 and Catalyst power

Note: Presentation applies to the ML505 and ML506
Extracting the Design

- Unzip the ml505_ibert_3gtps_design.zip file

Note: For the ML506, use the ml506_ibert_3gtps_design.zip file
ChipScope Setup

- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)

Note: Presentation applies to the ML505 and ML506
ChipScope Setup

- Select Device → DEV:4 MyDevice4 (XC5VLX50T) → Configure…
- Select <Design Path>\ml505_ibert_design.bit

Note: Presentation applies to the ML505 and ML506
ChipScope Setup

- Select File → Open Project...
- Select <Design Path>\ml505_ibert_design.cpj

**Note:** Presentation applies to the ML505 and ML506
Running IBERT

- Click Yes on this dialog box
IBERT ChipScope MGT Settings

- Set the Loopback mode to Near-End PCS for X0Y3_0
- Click on the Edit Line Rate button
IBERT ChipScope MGT Settings

- For GTP_DUAL_X0Y1 (PCIe), set the Target Line Rate to 2500

Note: Presentation applies to the ML505 and ML506
IBERT ChipScope MGT Settings

- For GTP_DUAL_X0Y3, set the Target Line Rate to 2500

Note: Presentation applies to the ML505 and ML506
IBERT ChipScope MGT Settings

• For GTP_DUAL_X0Y4, set the Target Line Rate to 3000

Note: Presentation applies to the ML505 and ML506
IBERT ChipScope TX Settings

- Diff Swing = 400mV; Pre-emphasis = 10%
IBERT ChipScope RX Settings

- Enable RX EQ Checked
IBERT ChipScope BERT Settings

- TX/RX Data Patterns set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)
Running IBERT

- View the RX Line Rate (1) and the RX Bit Error Count (2)
Documentation

• ML505/506
  – ML505 Overview
    http://www.xilinx.com/ml505
  – ML506 Overview
    http://www.xilinx.com/ml506
  – ML505/506 Getting Started Tutorial – UG348
  – ML505/506 Schematics
Documentation

• RocketIO
  – RocketIO GTP User Guide – UG196

• ChipScope Pro
  – ChipScope Pro 9.1i Serial IO Toolkit User Manual
    http://www.xilinx.com/ise/verification/chipscope_pro_siotk_9_1i_ug213.pdf
  – ChipScope Pro 9.1i User Manual
    http://www.xilinx.com/ise/verification/chipscope_pro_sw_cores_9_1i_ug029.pdf