ML505/506 SATA IBERT Design Creation
Using 9.1i SP3 ChipScope™ Pro

April 2007
ML505 IBERT Overview

• Software Requirements
• Design Generation
  – Highlighting the Virtex-5 RocketIO™ GTP Transceivers
Additional Setup Details

• Refer to ml505_overview_setup document for details on:
  – Software Requirements
  – ML505 Board Setup
    • Equipment and Cables
    • Software
    • Network
  – Terminal Programs
    • This presentation requires the 9600-8-N-1 Baud terminal setup

Note: This presentation can be used for ML505 or ML506; see notes at bottom of these pages
ChipScope Software Requirement

- Xilinx ChipScope 9.1i SP3
IBERT Generation

- Open the ChipScope Pro Core Generator
- Select IBERT
**IBERT Generation**

- Set the output to your design directory
- Make these settings:
  - Virtex5
  - xc5vlx50t
  - ff1136
  - -1

**Note:** For the ML506, use Device xc5vsx50t
IBERT Generation

- System Clock Settings:
  - I/O Std: LVCMOS33
  - P Source Pin: AH15
  - Set Freq: 100

Note: Presentation applies to the ML505 and ML506
IBERT Generation

- Select Enable GTP_DUAL_X0Y2
  - Set Max Line Rate to 1500
  - Set Ref Clock Frequency to 150
  - Set Pattern Settings as shown

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Note: Presentation applies to the ML505 and ML506
IBERT Generation

• Leave this screen as is
IBERT Generation

- Click Generate Design
IBERT Generation

- Bitstream is compiled and ready to use

Note: Presentation applies to the ML505 and ML506
Documentation

- ML505/506
  - ML505 Overview
    http://www.xilinx.com/ml505
  - ML506 Overview
    http://www.xilinx.com/ml506
  - ML505/506 User Guide – UG347
  - ML505/506 Getting Started Tutorial – UG348
  - ML505/506 Schematics
Documentation

• RocketIO
  – RocketIO GTP User Guide – UG196

• ChipScope Pro
  – ChipScope Pro 9.1i Serial IO Toolkit User Manual
    http://www.xilinx.com/ise/verification/chipscope_pro_siotk_9_1i_ug213.pdf
  – ChipScope Pro 9.1i User Manual
    http://www.xilinx.com/ise/verification/chipscope_pro_sw_cores_9_1i_ug029.pdf