



# ML507 Four GTXs IBERT Design Creation Using 10.1i SP2 ChipScope™ Pro

June 2008



# ML507 IBERT Overview

- Software Requirements
- Design Generation
  - Highlighting the Virtex-5 RocketIO™ GTX Transceivers

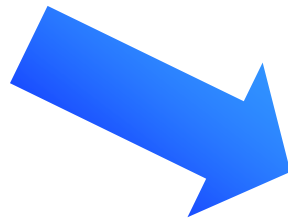
# Additional Setup Details

- Refer to ml505\_overview\_setup document for details on:
  - Software Requirements
  - ML507 Board Setup
    - **Equipment and Cables**
    - **Software**
    - **Network**
  - Terminal Programs
    - **This presentation requires the 9600-8-N-1 Baud terminal setup**



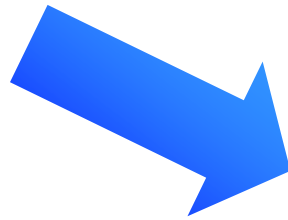
# ISE Software Requirement

- Xilinx ISE 10.1i SP2 software



# ChipScope Software Requirement

- Xilinx ChipScope Pro 10.1i SP2



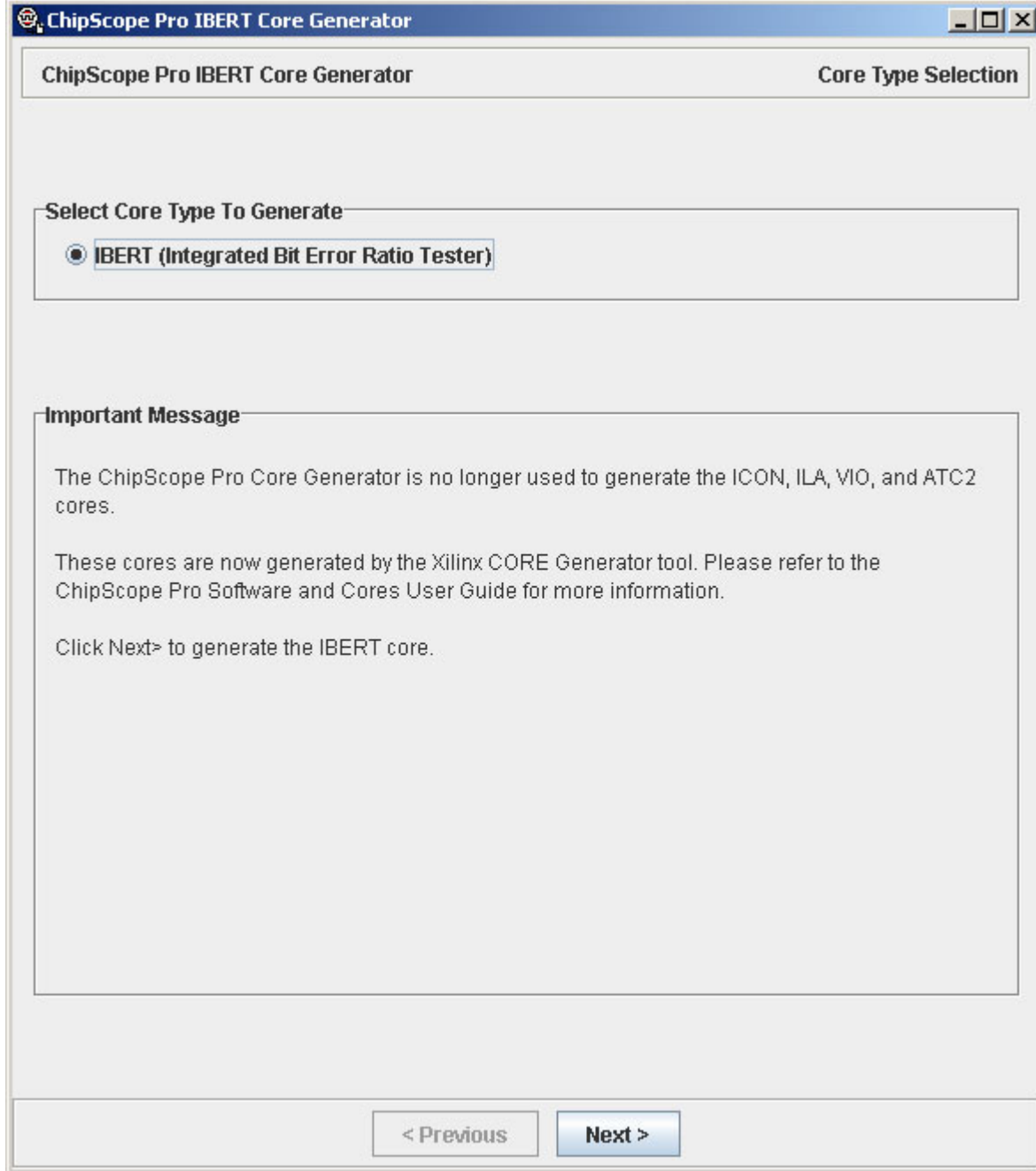
**ChipScope Pro IBERT Core Generator**

Release Version: 10.1 02  
Application Version: K.37 (Build 10102.8.151.695)  
Copyright (c) 1995-2008 Xilinx, Inc.  
All rights reserved.

# IBERT Generation

- Open the ChipScope Pro IBERT Core Generator



# IBERT Generation

- Set the output to your design directory
- Make these settings:
  - Virtex5
  - xc5vfx70t
  - ff1136
  - -1

ChipScope Pro IBERT Core Generator

IBERT General Options

Design Files

Output Bitstream: C:\ml507\_ibert\_4gbxs\ml507\_ibert\_design.bit Browse

Device Selection

Device Family: Virtex5

Device: xc5vfx70t

Package: ff1136

Speed Grade: -1

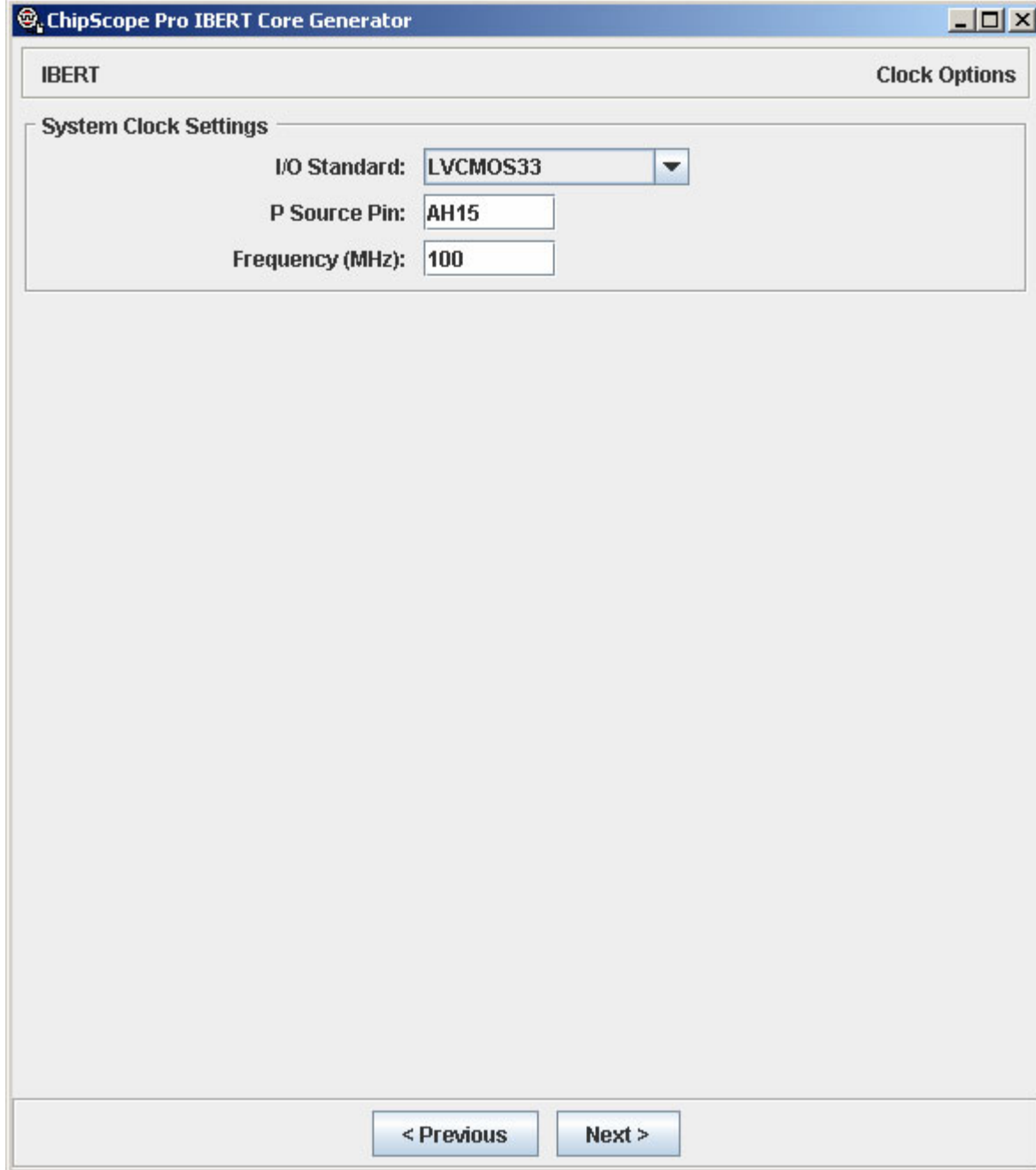
Silicon Revision

Silicon Revision: Production

< Previous Next >

# IBERT Generation

- System Clock Settings:
  - I/O Std: LVCMOS33
  - P Source Pin: AH15
  - Set Freq: 100



The screenshot shows the 'ChipScope Pro IBERT Core Generator' window. The title bar includes the application name and standard window controls. The main window has a header 'IBERT' and a 'Clock Options' button. Below this is a 'System Clock Settings' section with three input fields: 'I/O Standard' set to 'LVCMOS33', 'P Source Pin' set to 'AH15', and 'Frequency (MHz)' set to '100'. At the bottom of the window are two buttons: '< Previous' and 'Next >'.

# IBERT Generation

- Set the Pattern Settings as shown

The screenshot shows the 'ChipScope Pro IBERT Core Generator' window. The title bar includes the application name and standard window controls. The main window is titled 'IBERT' and has a 'MGT Options' button in the top right corner.

**Resource Usage:**  
Number of GTX Duals used: 0 out of 8  
Number of DCMs used: 0 out of 12

**Pattern Settings:** A list of checkboxes is shown, with a red box highlighting the first eight options:  PRBS 7-bit,  PRBS 7-bit Alt,  PRBS 9-bit,  PRBS 11-bit,  PRBS 15-bit,  PRBS 20-bit,  PRBS 23-bit, and  PRBS 29-bit. Below these are  PRBS 31-bit,  User Pattern,  Framed Counter, and  Idle Pattern.

**GTX Settings:** Two sections are visible. The first is for 'Enable GTX\_DUAL\_X0Y0 (MGT126)'. It shows 'Ref Clock Pins (P, N): AL7, AM7'. Below this is a table for TX and RX pins:

GTX	TX Pins (P, N)	RX Pins (P, N)
GTX 0:	AN5, AN6	AP6, AP7
GTX 1:	AN10, AN9	AP9, AP8

Below the table are fields for 'Frequency Mode: Invalid Line Rate', 'Max Line Rate (Mbps):', and 'Ref Clock Freq (MHz):'. The second section is for 'Enable GTX\_DUAL\_X0Y1 (MGT122)'. It shows 'Ref Clock Pins (P, N): AL5, AL4'. Below this is a table for TX and RX pins:

GTX	TX Pins (P, N)	RX Pins (P, N)
GTX 0:	AK2, AL2	AL1, AM1
GTX 1:	AN4, AN3	AP3, AP2

Below the table are fields for 'Frequency Mode: Invalid Line Rate', 'Max Line Rate (Mbps):', and 'Ref Clock Freq (MHz):'. At the bottom of the window are '< Previous' and 'Next >' buttons.

# IBERT Generation

- Select Enable GTX\_DUAL\_X0Y2
  - Set Max Line Rate to 2500
  - Set Ref Clock Frequency to 100
- Select Enable GTX\_DUAL\_X0Y3
  - Set Max Line Rate to 3000
  - Set Ref Clock Frequency to 150

The screenshot shows the 'IBERT' configuration window in the ChipScope Pro IBERT Core Generator. The window is divided into several sections:

- Resource Usage:** Number of GTX Duals used: 2 out of 8; Number of DCMs used: 6 out of 12.
- Pattern Settings:** A list of checkboxes for various PRBS patterns and other settings:
  - PRBS 7-bit
  - PRBS 7-bit Alt
  - PRBS 9-bit
  - PRBS 11-bit
  - PRBS 15-bit
  - PRBS 20-bit
  - PRBS 23-bit
  - PRBS 29-bit
  - PRBS 31-bit
  - User Pattern
  - Framed Counter
  - Idle Pattern
- GTX Settings:** Two sections for configuring GTX\_DUAL\_X0Y2 (MGT118) and GTX\_DUAL\_X0Y3 (MGT114).
  - GTX\_DUAL\_X0Y2 (MGT118):**
    - Enable GTX\_DUAL\_X0Y2 (MGT118):
    - Ref Clock Pins (P, N): AF4, AF3
    - TX Pins (P, N): GTX 0: AD2, AE2; GTX 1: AJ2, AH2
    - RX Pins (P, N): AE1, AF1; AH1, AG1
    - Frequency Mode: High Freq (2400Mbps - 6500Mbps)
    - Max Line Rate (Mbps): 2500
    - Ref Clock Freq (MHz): 100.000 (FB=5, REF=1, DIVSEL=2)
  - GTX\_DUAL\_X0Y3 (MGT114):**
    - Enable GTX\_DUAL\_X0Y3 (MGT114):
    - Ref Clock Pins (P, N): Y4, Y3
    - TX Pins (P, N): GTX 0: V2, W2; GTX 1: AC2, AB2
    - RX Pins (P, N): W1, Y1; AB1, AA1
    - Frequency Mode: High Freq (2400Mbps - 6500Mbps)
    - Max Line Rate (Mbps): 3000
    - Ref Clock Freq (MHz): 150.000 (FB=4, REF=1, DIVSEL=2)

At the bottom of the window, there are navigation buttons: '< Previous' and 'Next >'.

# IBERT Generation

- Select Enable GTX\_DUAL\_X0Y4
  - Set Max Line Rate to 2500
  - Set Ref Clock Frequency to 125
- Select Enable GTX\_DUAL\_X0Y5
  - Set Max Line Rate to 3000
  - Set Ref Clock Frequency to 150

The screenshot shows the 'ChipScope Pro IBERT Core Generator' window. The title bar includes the Xilinx logo and the text 'ChipScope Pro IBERT Core Generator'. The window is divided into several sections:

- IBERT** (top left) and **MGT Options** (top right).
- Resource Usage**: Number of GTX Duals used: 4 out of 8; Number of DCMs used: 12 out of 12.
- Pattern Settings**: A list of checkboxes for PRBS patterns (7-bit, 7-bit Alt, 9-bit, 11-bit, 15-bit, 20-bit, 23-bit, 29-bit, 31-bit), User Pattern, Framed Counter, and Idle Pattern. All are checked.
- GTX Settings**: Two configuration panels for GTX\_DUAL\_X0Y4 (MGT112) and GTX\_DUAL\_X0Y5 (MGT116).
  - GTX\_DUAL\_X0Y4 (MGT112)**:
    - Enable GTX\_DUAL\_X0Y4 (MGT112) [checked]
    - Ref Clock Pins (P, N): P4, P3
    - TX Pins (P, N): GTX 0: M2, N2; GTX 1: U2, T2
    - RX Pins (P, N): N1, P1; T1, R1
    - Frequency Mode: High Freq (2400Mbps - 6500Mbps)
    - Max Line Rate (Mbps): 2500
    - Ref Clock Freq (MHz): 125.000 (FB=4, REF=1, DIVSEL=2)
  - GTX\_DUAL\_X0Y5 (MGT116)**:
    - Enable GTX\_DUAL\_X0Y5 (MGT116) [checked]
    - Ref Clock Pins (P, N): H4, H3
    - TX Pins (P, N): GTX 0: F2, G2; GTX 1: L2, K2
    - RX Pins (P, N): G1, H1; K1, J1
    - Frequency Mode: High Freq (2400Mbps - 6500Mbps)
    - Max Line Rate (Mbps): 3000
    - Ref Clock Freq (MHz): 150.000 (FB=4, REF=1, DIVSEL=2)
- Navigation buttons: < Previous and Next >

# IBERT Generation

- Leave this screen as is



# IBERT Generation

- Click Generate Design



# IBERT Generation

- Bitstream is compiled and ready to use

The screenshot displays the 'ChipScope Pro IBERT Core Generator' window. The title bar includes the application name and standard window controls. The main area is titled 'IBERT' and 'Core Generation'. A 'Messages' pane shows the following text:

```
Creating Design Bitstream (step 6 of 6)  
  
Running: bitgen -intstyle silent -d -w -g StartUpClk:JTAGCLK -g UnusedPin:Pullnone  
ml507_ibert_design_top.ncd ml507_ibert_design.bit  
Directory: C:\ml507_ibert_4gbx\libertgbx_temp  
Start Time: Thu Jun 12 18:59:14 GMT-06:00 2008  
  
Please wait .....  
  
End Time: Thu Jun 12 19:01:18 GMT-06:00 2008  
Step 6 Elapsed Time: 00:02:03  
Total Elapsed Time: 01:13:32  
  
* Creating Design Bitstream Completed *  
=====
```

Below this, another summary message is shown:

```
=====
```

```
* IBERT Design Generation Completed *  
  
Start Time: Thu Jun 12 17:47:45 GMT-06:00 2008  
End Time: Thu Jun 12 19:01:18 GMT-06:00 2008  
  
Step 1 Run Time: 00:01:51  
Step 2 Run Time: 00:30:23  
Step 3 Run Time: 00:00:59  
Step 4 Run Time: 00:29:53  
Step 5 Run Time: 00:08:19  
Step 6 Run Time: 00:02:03  
Total Elapsed Run Time: 01:13:32  
=====
```

At the bottom of the window, there are three buttons: '< Previous', 'Cancel', and 'Start Over'.

# Documentation

- Virtex-5
  - Silicon Devices  
[http://www.xilinx.com/products/silicon\\_solutions](http://www.xilinx.com/products/silicon_solutions)
  - Virtex-5 Multi-Platform FPGA  
[http://www.xilinx.com/products/silicon\\_solutions/fpgas/virtex/virtex5](http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5)
  - Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds100.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf)
  - Virtex-5 FPGA DC and Switching Characteristics Data Sheet  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds202.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf)

# Documentation

- Virtex-5
  - Virtex-5 FPGA User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug190.pdf](http://www.xilinx.com/support/documentation/user_guides/ug190.pdf)
  - Virtex-5 FPGA Configuration User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug191.pdf](http://www.xilinx.com/support/documentation/user_guides/ug191.pdf)
  - Virtex-5 System Monitor User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug192.pdf](http://www.xilinx.com/support/documentation/user_guides/ug192.pdf)
  - Virtex-5 Packaging and Pinout Specification  
[http://www.xilinx.com/support/documentation/user\\_guides/ug195.pdf](http://www.xilinx.com/support/documentation/user_guides/ug195.pdf)

# Documentation

- Virtex-5 RocketIO
  - RocketIO GTP Transceivers  
[http://www.xilinx.com/products/silicon\\_solutions/fpgas/virtex/virtex5/capabilities/RocketIO\\_GTP.htm](http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTP.htm)
  - RocketIO GTX Transceivers  
[http://www.xilinx.com/products/silicon\\_solutions/fpgas/virtex/virtex5/capabilities/RocketIO\\_GTX.htm](http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTX.htm)
  - RocketIO GTP Transceiver User Guide – UG196  
[http://www.xilinx.com/support/documentation/user\\_guides/ug196.pdf](http://www.xilinx.com/support/documentation/user_guides/ug196.pdf)
  - RocketIO GTX Transceiver User Guide – UG198  
[http://www.xilinx.com/support/documentation/user\\_guides/ug198.pdf](http://www.xilinx.com/support/documentation/user_guides/ug198.pdf)

# Documentation

- Design Resources

- ISE Development Tools and IP

<http://www.xilinx.com/ise>

- Integrated Software Environment (ISE) Foundation Resources

[http://www.xilinx.com/ise/logic\\_design\\_prod/foundation.htm](http://www.xilinx.com/ise/logic_design_prod/foundation.htm)

- ISE Manuals

[http://www.xilinx.com/support/software\\_manuals.htm](http://www.xilinx.com/support/software_manuals.htm)

- ISE Development System Reference Guide

<http://toolbox.xilinx.com/docsan/xilinx10/books/docs/dev/dev.pdf>

- ISE Development System Libraries Guide

[http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5\\_hdl/virtex5\\_hdl.pdf](http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5_hdl/virtex5_hdl.pdf)

# Documentation

- Additional Design Resources
  - Customer Support  
<http://www.xilinx.com/support>
  - Xilinx Design Services:  
<http://www.xilinx.com/xds>
  - Titanium Dedicated Engineering:  
<http://www.xilinx.com/titanium>
  - Education Services:  
<http://www.xilinx.com/education>
  - Xilinx On Board (Board and kit locator):  
<http://www.xilinx.com/xob>

# Documentation

- ChipScope Pro
  - ChipScope Pro 10.1i Serial IO Toolkit User Manual  
[http://www.xilinx.com/ise/verification/chipscope\\_pro\\_siotk\\_10\\_1\\_ug213.pdf](http://www.xilinx.com/ise/verification/chipscope_pro_siotk_10_1_ug213.pdf)
  - ChipScope Pro 10.1i ChipScope Pro Software and Cores User Guide  
[http://www.xilinx.com/ise/verification/chipscope\\_pro\\_sw\\_cores\\_10\\_1\\_ug029.pdf](http://www.xilinx.com/ise/verification/chipscope_pro_sw_cores_10_1_ug029.pdf)

# Documentation

- Ethernet

- Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet

[http://www.xilinx.com/support/documentation/ip\\_documentation/v5\\_emac\\_ds550.pdf](http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_ds550.pdf)

- Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide

[http://www.xilinx.com/support/documentation/ip\\_documentation/v5\\_emac\\_gsg340.pdf](http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_gsg340.pdf)

- Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide

[http://www.xilinx.com/support/documentation/user\\_guides/ug194.pdf](http://www.xilinx.com/support/documentation/user_guides/ug194.pdf)

- LightWeight IP (lwIP) Application Examples – XAPP1026

[http://www.xilinx.com/support/documentation/application\\_notes/xapp1026.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp1026.pdf)

# Documentation

- PCIe
  - LogiCORE Endpoint Block Plus for PCI Express Data Sheet  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_ds551.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ds551.pdf)
  - LogiCORE Endpoint Block Plus for PCI Express Designs  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_ug341.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ug341.pdf)
  - LogiCORE Endpoint Block Plus Getting Started Guide for PCI Express Designs  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_gsg343.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_gsg343.pdf)
  - Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs  
[http://www.xilinx.com/support/documentation/user\\_guides/ug197.pdf](http://www.xilinx.com/support/documentation/user_guides/ug197.pdf)

# Documentation

- ML505/506/507
  - ML505 Overview  
<http://www.xilinx.com/ml505>
  - ML506 Overview  
<http://www.xilinx.com/ml506>
  - ML507 Overview  
<http://www.xilinx.com/ml507>
  - ML505/506/507 Evaluation Platform User Guide – UG347  
[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug347.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug347.pdf)
  - ML505/506/507 Getting Started Tutorial – UG348  
[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug348.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug348.pdf)
  - ML505/506/507 Reference Design User Guide – UG349  
[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug349.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug349.pdf)

# Documentation

- ML505/506/507

- ML505/506/507 Schematics

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ml50x\\_schematics.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ml50x_schematics.pdf)

- ML505/506/507 Bill of Material

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ml505\\_501\\_bom.xls](http://www.xilinx.com/support/documentation/boards_and_kits/ml505_501_bom.xls)