



# **ML507 Four GTXs IBERT Design Creation Using 11.1 ChipScope™ Pro**

**May 2009**

# ML507 IBERT Overview

- **Software Requirements**
- **Design Generation**
  - Highlighting the Virtex-5 RocketIO™ GTX Transceivers
- **References**

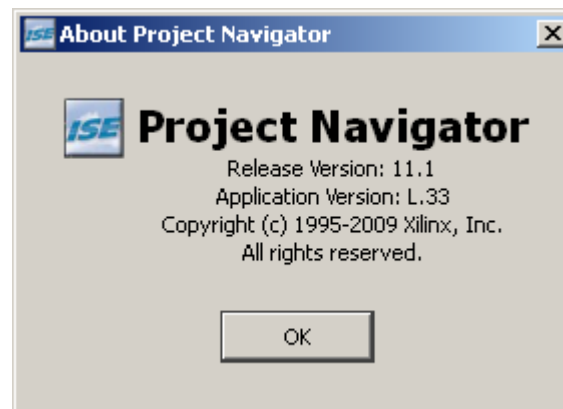
# Additional Setup Details

- **Refer to [ml505\\_overview\\_setup.ppt](#) for details on:**
  - Software Requirements
  - ML507 Board Setup
  - Equipment and Cables
  - Software
  - Network



# ISE Software Requirement

- Xilinx ISE 11.1 software



# ChipScope Pro Software Requirement

- Xilinx ChipScope Pro 11.1 software



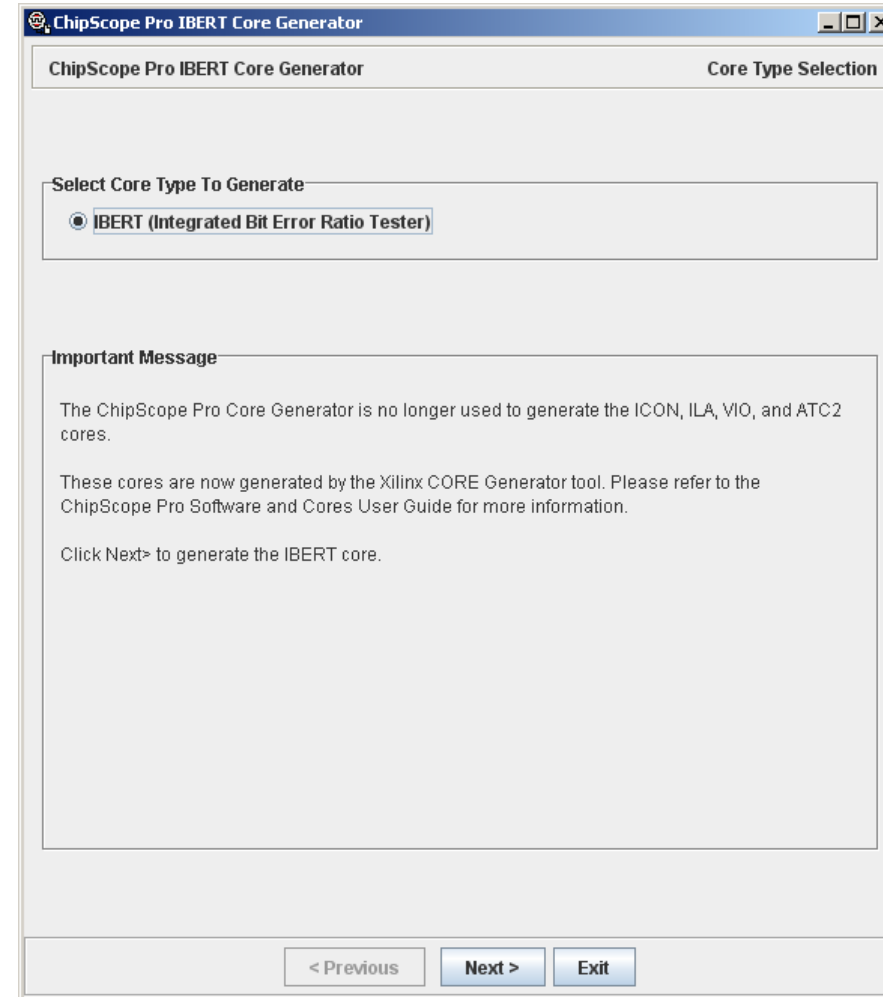
**ChipScope Pro Analyzer**

Release Version: 11.1  
Application Version:  
Copyright (c) 1995-2008 Xilinx, Inc.  
All rights reserved.

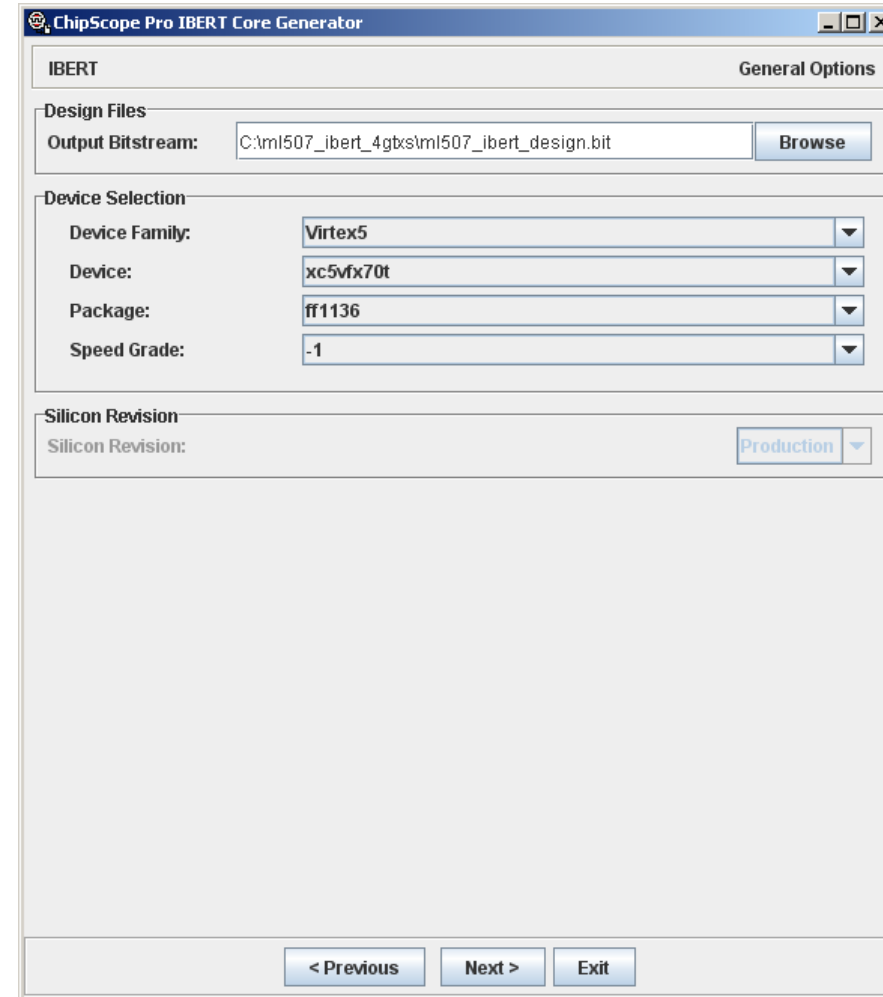
# IBERT Generation

- Open the ChipScope Pro IBERT Core Generator



# IBERT Generation

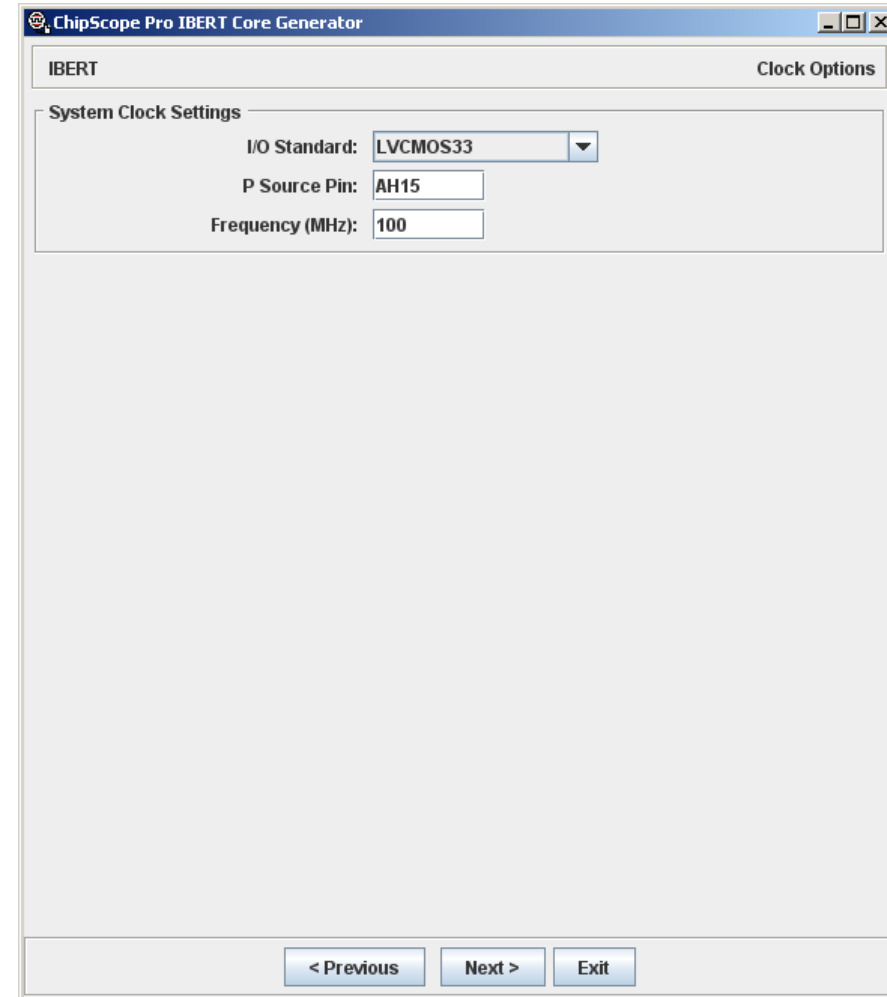
- Set the output to your design directory
- Make these settings:
  - Virtex5
  - xc5vfx70t
  - ff1136
  - -1



# IBERT Generation

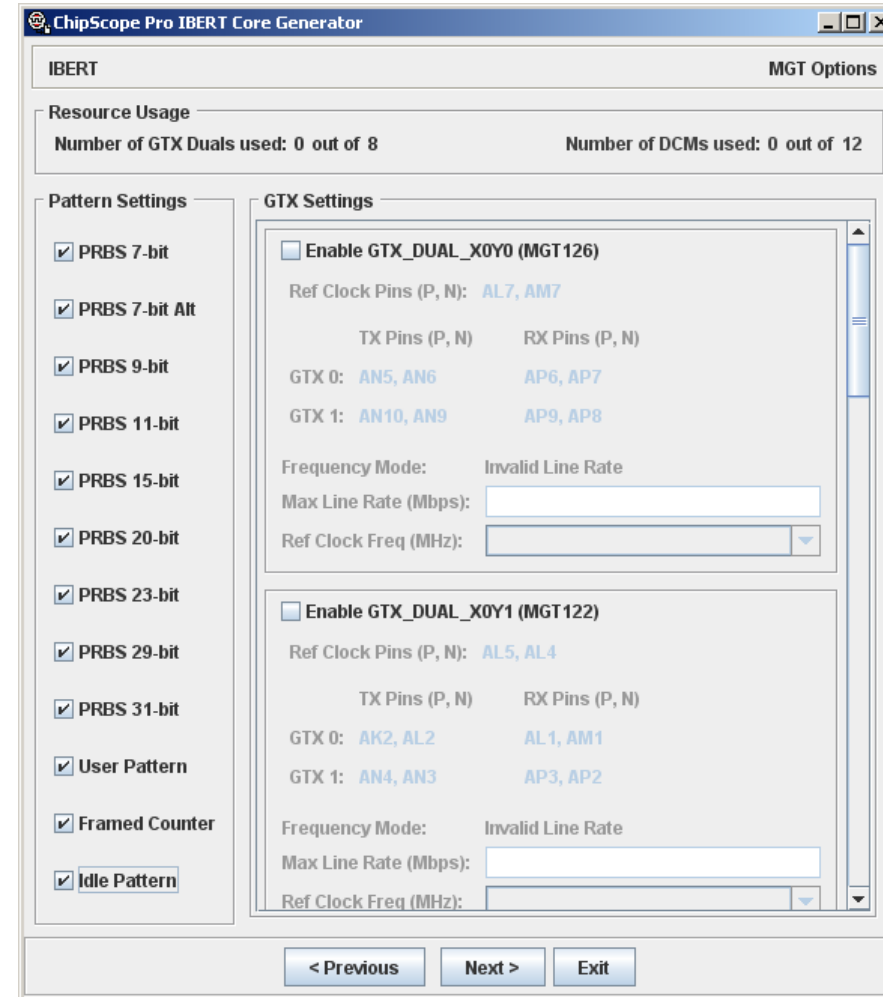
## ■ System Clock Settings:

- I/O Std: LVCMOS33
- P Source Pin: AH15
- Set Freq: 100



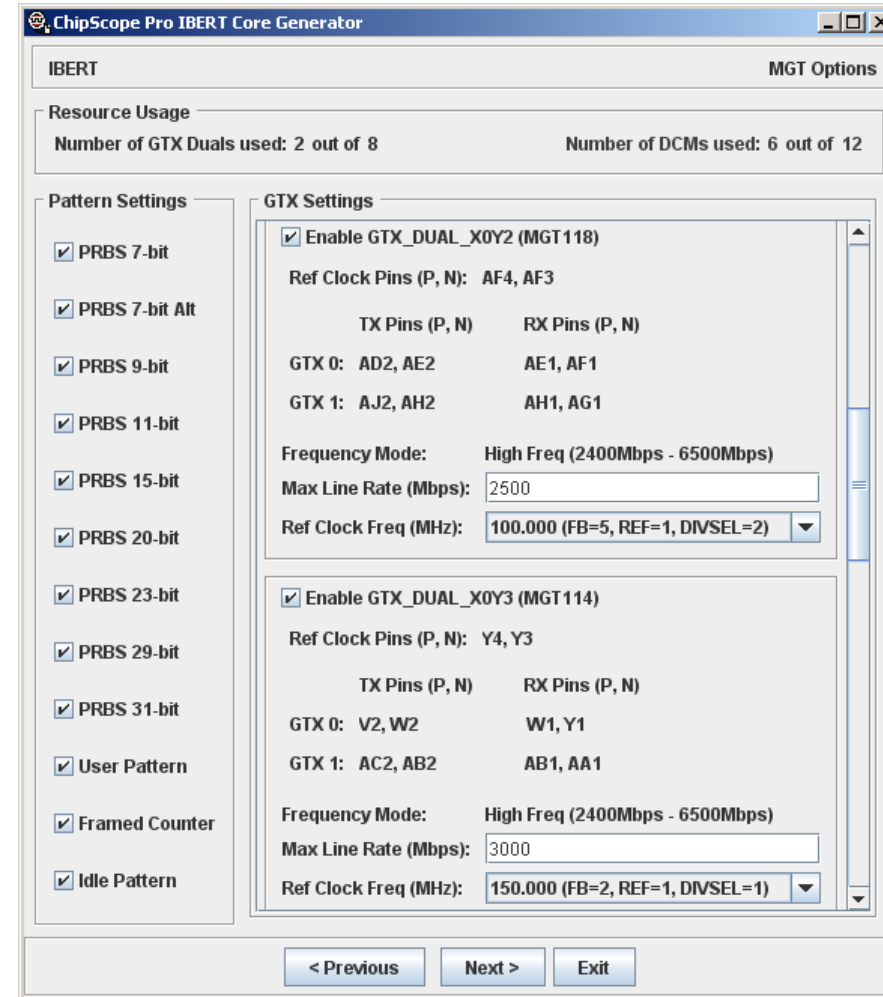
# IBERT Generation

- Set the Pattern Settings as shown



# IBERT Generation

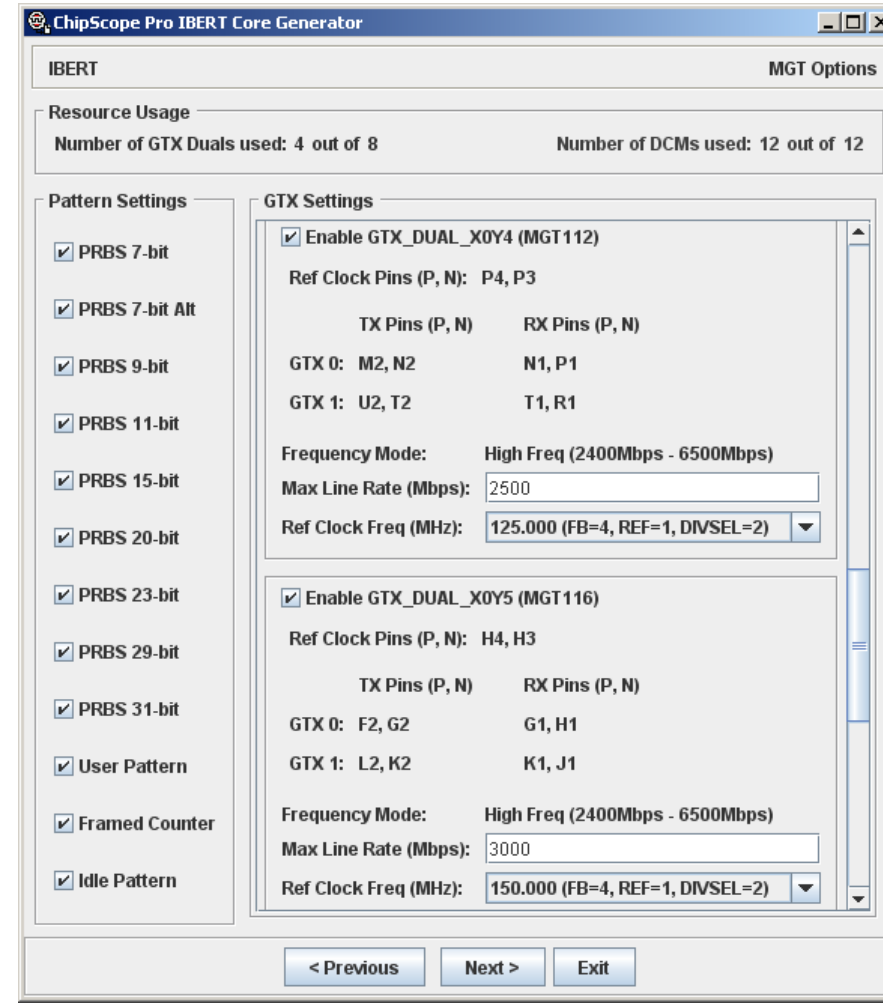
- **Select Enable GTX\_DUAL\_X0Y2**
  - Set Max Line Rate to 2500
  - Set Ref Clock Frequency to 100
- **Select Enable GTX\_DUAL\_X0Y3**
  - Set Max Line Rate to 3000
  - Set Ref Clock Frequency to 150



**Note:** GTX\_DUAL\_X0Y2 = PCIe; GTX\_DUAL\_X0Y3 = SATA

# IBERT Generation

- **Select Enable GTX\_DUAL\_X0Y4**
  - Set Max Line Rate to 2500
  - Set Ref Clock Frequency to 125
- **Select Enable GTX\_DUAL\_X0Y5**
  - Set Max Line Rate to 3000
  - Set Ref Clock Frequency to 150



**Note:** GTX\_DUAL\_X0Y4 = SGMII; GTX\_DUAL\_X0Y5 = SFP, SMA

# IBERT Generation

- Leave this screen as is



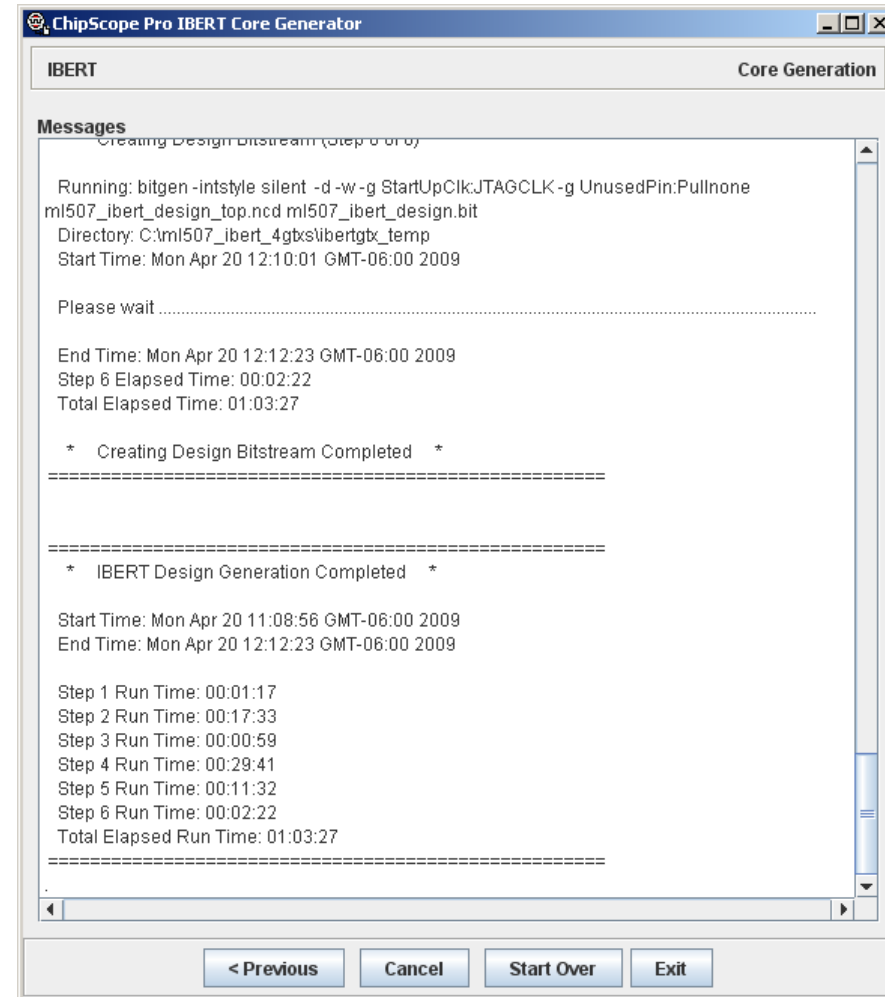
# IBERT Generation

- Click Generate Design



# IBERT Generation

- Bitstream is compiled and ready to use



The screenshot shows the 'ChipScope Pro IBERT Core Generator' window. The title bar includes the application name and standard window controls. The main area is titled 'IBERT' and 'Core Generation'. A 'Messages' pane displays the following text:

```
Creating Design Bitstream (step 6 of 6)

Running: bitgen -intstyle silent -d -w -g StartUpClk:JTAGCLK -g UnusedPin:Pullnone
ml507_ibert_design_top.ncd ml507_ibert_design.bit
Directory: C:\ml507_ibert_4gbs\libertgbx_temp
Start Time: Mon Apr 20 12:10:01 GMT-06:00 2009

Please wait .....

End Time: Mon Apr 20 12:12:23 GMT-06:00 2009
Step 6 Elapsed Time: 00:02:22
Total Elapsed Time: 01:03:27

* Creating Design Bitstream Completed *
```

Below this, a summary of the entire process is shown:

```
=====

* IBERT Design Generation Completed *

Start Time: Mon Apr 20 11:08:56 GMT-06:00 2009
End Time: Mon Apr 20 12:12:23 GMT-06:00 2009

Step 1 Run Time: 00:01:17
Step 2 Run Time: 00:17:33
Step 3 Run Time: 00:00:59
Step 4 Run Time: 00:29:41
Step 5 Run Time: 00:11:32
Step 6 Run Time: 00:02:22
Total Elapsed Run Time: 01:03:27

=====
```

At the bottom of the window, there are four buttons: '< Previous', 'Cancel', 'Start Over', and 'Exit'.

# References

# Documentation

## ▪ ChipScope Pro

- ChipScope Pro 10.1i Serial IO Toolkit User Manual

[http://www.xilinx.com/ise/verification/chipscope\\_pro\\_siotk\\_10\\_1\\_ug213.pdf](http://www.xilinx.com/ise/verification/chipscope_pro_siotk_10_1_ug213.pdf)

- ChipScope Pro 11.1 ChipScope Pro Software and Cores User Guide

<http://www.xilinx.com/support/documentation/>

[sw\\_manufactures/xilinx11/chipscope\\_pro\\_sw\\_cores\\_11\\_1\\_ug029.pdf](http://www.xilinx.com/support/documentation/sw_manufactures/xilinx11/chipscope_pro_sw_cores_11_1_ug029.pdf)

# Additional Documentation

# Documentation

## ▪ Virtex-5

- Silicon Devices

<http://www.xilinx.com/products/devices.htm>

- Virtex-5 Multi-Platform FPGA

<http://www.xilinx.com/products/virtex5/index.htm>

- Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms

[http://www.xilinx.com/support/documentation/data\\_sheets/ds100.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf)

- Virtex-5 FPGA DC and Switching Characteristics Data Sheet

[http://www.xilinx.com/support/documentation/data\\_sheets/ds202.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf)

# Documentation

## ▪ Virtex-5

- Virtex-5 FPGA User Guide

[http://www.xilinx.com/support/documentation/user\\_guides/ug190.pdf](http://www.xilinx.com/support/documentation/user_guides/ug190.pdf)

- Virtex-5 FPGA Configuration User Guide

[http://www.xilinx.com/support/documentation/user\\_guides/ug191.pdf](http://www.xilinx.com/support/documentation/user_guides/ug191.pdf)

- Virtex-5 System Monitor User Guide

[http://www.xilinx.com/support/documentation/user\\_guides/ug192.pdf](http://www.xilinx.com/support/documentation/user_guides/ug192.pdf)

- Virtex-5 Packaging and Pinout Specification

[http://www.xilinx.com/support/documentation/user\\_guides/ug195.pdf](http://www.xilinx.com/support/documentation/user_guides/ug195.pdf)

# Documentation

## ▪ Virtex-5 RocketIO

- RocketIO GTP Transceivers

<http://www.xilinx.com/products/virtex5/lxt.htm>

- RocketIO GTP Transceiver User Guide – UG196

[http://www.xilinx.com/support/documentation/user\\_guides/ug196.pdf](http://www.xilinx.com/support/documentation/user_guides/ug196.pdf)

- RocketIO GTX Transceivers

<http://www.xilinx.com/products/virtex5/fxt.htm>

- RocketIO GTX Transceiver User Guide – UG198

[http://www.xilinx.com/support/documentation/user\\_guides/ug198.pdf](http://www.xilinx.com/support/documentation/user_guides/ug198.pdf)

# Documentation

## ▪ Design Resources

- IDS - ISE Design Suite

<http://www.xilinx.com/tools/designtools.htm>

- ISE Manuals

[http://www.xilinx.com/support/documentation/dt\\_ise11-1.htm](http://www.xilinx.com/support/documentation/dt_ise11-1.htm)

- ISE Command Line Tools User Guide

[http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx11/devref.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/devref.pdf)

- ISE Development System Libraries Guide

[http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx11/virtex5\\_hdl.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/virtex5_hdl.pdf)

# Documentation

## ▪ Additional Design Resources

- Customer Support

<http://www.xilinx.com/support>

- Xilinx Design Services:

<http://www.xilinx.com/xds>

- Titanium Dedicated Engineering:

<http://www.xilinx.com/titanium>

- Education Services:

<http://www.xilinx.com/education>

- Xilinx On Board (Board and kit locator):

<http://www.xilinx.com/products/devkits/boardsearch.htm>

# Documentation

## ▪ Platform Studio

- Embedded Development Kit (EDK) Resources

<http://www.xilinx.com/tools/platform.htm>

- Embedded System Tools Reference Manual

[http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx11/est\\_rm.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/est_rm.pdf)

- EDK Concepts, Tools, and Techniques

[http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx11/edk\\_ctt.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/edk_ctt.pdf)

# Documentation

## ▪ PowerPC 440

- Embedded Processor Block in Virtex-5 FPGAs Reference Guide – UG200  
[http://www.xilinx.com/support/documentation/user\\_guides/ug200.pdf](http://www.xilinx.com/support/documentation/user_guides/ug200.pdf)
- PPC440 Virtex-5 Wrapper – DS621  
[http://www.xilinx.com/support/documentation/ip\\_documentation/ppc440\\_virtex5.pdf](http://www.xilinx.com/support/documentation/ip_documentation/ppc440_virtex5.pdf)
- DDR2 Memory Controller for PowerPC 440 Processors – DS567  
[http://www.xilinx.com/support/documentation/ip\\_documentation/ppc440mc\\_ddr2.pdf](http://www.xilinx.com/support/documentation/ip_documentation/ppc440mc_ddr2.pdf)

# Documentation

- **MicroBlaze**

- MicroBlaze Processor

- <http://www.xilinx.com/tools/microblaze.htm>

- MicroBlaze Processor Reference Guide – UG081

- [http://www.xilinx.com/support/documentation/sw\\_manufactures/mb\\_ref\\_guide.pdf](http://www.xilinx.com/support/documentation/sw_manufactures/mb_ref_guide.pdf)

# Documentation

## ▪ ChipScope Pro

- ChipScope Pro 10.1i Serial IO Toolkit User Manual

[http://www.xilinx.com/ise/verification/chipscope\\_pro\\_siotk\\_10\\_1\\_ug213.pdf](http://www.xilinx.com/ise/verification/chipscope_pro_siotk_10_1_ug213.pdf)

- ChipScope Pro 11.1 ChipScope Pro Software and Cores User Guide

[http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx11/chipscope\\_pro\\_sw\\_cores\\_11\\_1\\_ug029.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/chipscope_pro_sw_cores_11_1_ug029.pdf)

# Documentation

## ▪ Memory Solutions

- Demos on Demand – Memory Interface Solutions with Xilinx FPGAs  
[http://www.demosondemand.com/clients/xilinx/001/page\\_new2/index.asp#35](http://www.demosondemand.com/clients/xilinx/001/page_new2/index.asp#35)
- Xilinx Memory Corner  
[http://www.xilinx.com/products/design\\_resources/mem\\_corner](http://www.xilinx.com/products/design_resources/mem_corner)
- Additional Memory Resources  
<http://www.xilinx.com/support/software/memory/protected/index.htm>
- Xilinx Memory Interface Generator (MIG) 3.0 User Guide  
[http://www.xilinx.com/support/documentation/ip\\_documentation/ug086.pdf](http://www.xilinx.com/support/documentation/ip_documentation/ug086.pdf)
- Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator  
[http://www.xilinx.com/support/documentation/white\\_papers/wp260.pdf](http://www.xilinx.com/support/documentation/white_papers/wp260.pdf)

# Documentation

## ▪ Ethernet

- Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet  
[http://www.xilinx.com/support/documentation/ip\\_documentation/v5\\_emac\\_ds550.pdf](http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_ds550.pdf)
- Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide  
[http://www.xilinx.com/support/documentation/ip\\_documentation/v5\\_emac\\_gsg340.pdf](http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_gsg340.pdf)
- Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug194.pdf](http://www.xilinx.com/support/documentation/user_guides/ug194.pdf)
- LightWeight IP (lwIP) Application Examples – XAPP1026  
[http://www.xilinx.com/support/documentation/application\\_notes/xapp1026.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp1026.pdf)

# Documentation

## ▪ PCIe

- LogiCORE Endpoint Block Plus for PCI Express Data Sheet  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_ds551.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ds551.pdf)
- LogiCORE Endpoint Block Plus for PCI Express Designs  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_ug341.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ug341.pdf)
- LogiCORE Endpoint Block Plus Getting Started Guide for PCI Express Designs  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_gsg343.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_gsg343.pdf)
- Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs  
[http://www.xilinx.com/support/documentation/user\\_guides/ug197.pdf](http://www.xilinx.com/support/documentation/user_guides/ug197.pdf)

# Documentation

## ▪ System Generator

- System Generator for DSP

<http://www.xilinx.com/tools/sysgen.htm>

- Xilinx System Generator for DSP Getting Started Guide – UG639

[http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx11/sysgen\\_ref.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/sysgen_ref.pdf)

- Xilinx System Generator for DSP Getting Started Guide – UG639

[http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx11/sysgen\\_gs.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/sysgen_gs.pdf)

- Virtex-5 XtremeDSP Design Considerations User Guide – UG193

[http://www.xilinx.com/support/documentation/user\\_guides/ug193.pdf](http://www.xilinx.com/support/documentation/user_guides/ug193.pdf)

# Documentation

## ▪ PLB v4.6 IP

- Processor Local Bus (PLB) v4.6 – DS531

[http://www.xilinx.com/support/documentation/ip\\_documentation/plb\\_v46.pdf](http://www.xilinx.com/support/documentation/ip_documentation/plb_v46.pdf)

- Multi-Port Memory Controller (MPMC) – DS643

[http://www.xilinx.com/support/documentation/ip\\_documentation/mpmc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/mpmc.pdf)

- XPS Multi-Channel External Memory Controller (XPS MCH EMC) – DS575

[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_mch\\_emc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_mch_emc.pdf)

- XPS LocalLink TEMAC – DS537

[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_ll\\_temac.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_temac.pdf)

# Documentation

## ▪ PLB v4.6 IP

- XPS LocalLink FIFO – DS568

[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_ll\\_fifo.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_fifo.pdf)

- XPS IIC Bus Interface – DS606

[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_iic.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_iic.pdf)

- XPS SYSACE (System ACE) Interface Controller – DS583

[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_sysace.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_sysace.pdf)

- XPS Timer/Counter – DS573

[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_timer.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_timer.pdf)

# Documentation

## ▪ PLB v4.6 IP

- XPS Interrupt Controller – DS572

[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_intc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_intc.pdf)

- Using and Creating Interrupt-Based Systems Application Note

[http://www.xilinx.com/support/documentation/application\\_notes/xapp778.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp778.pdf)

- XPS General Purpose Input/Output (GPIO) – DS569

[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_gpio.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_gpio.pdf)

- XPS External Peripheral Controller (EPC) – DS581

[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_epc.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_epc.pdf)

# Documentation

## ▪ PLB v4.6 IP

- XPS 16550 UART – DS577

[http://www.xilinx.com/support/documentation/ip\\_documentation/xps\\_uart16550.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_uart16550.pdf)

- XPS Thin Film Transistor (TFT) Controller – DS695

[www.xilinx.com/support/documentation/ip\\_documentation/xps\\_tft.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_tft.pdf)

- XPS PS2 Controller – DS707

[www.xilinx.com/support/documentation/ip\\_documentation/xps\\_ps2.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_ps2.pdf)

- XPS Block RAM (BRAM) Interface Controller – DS596

[www.xilinx.com/support/documentation/ip\\_documentation/xps\\_bram\\_if\\_cntlr.pdf](http://www.xilinx.com/support/documentation/ip_documentation/xps_bram_if_cntlr.pdf)

# Documentation

## ▪ OPB Bridge IP

- PLBV46 to OPB Bridge – DS403

[http://www.xilinx.com/support/documentation/ip\\_documentation/plbv46\\_opb\\_bridge.pdf](http://www.xilinx.com/support/documentation/ip_documentation/plbv46_opb_bridge.pdf)

- On-Chip Peripheral Bus V2.0 with OPB Arbiter – DS401

[http://www.xilinx.com/support/documentation/ip\\_documentation/opb\\_v20.pdf](http://www.xilinx.com/support/documentation/ip_documentation/opb_v20.pdf)

# Documentation

## ▪ IP

- Local Memory Bus – DS445

[http://www.xilinx.com/support/documentation/ip\\_documentation/lmb\\_v10.pdf](http://www.xilinx.com/support/documentation/ip_documentation/lmb_v10.pdf)

- Block RAM Block – DS444

[http://www.xilinx.com/support/documentation/ip\\_documentation/bram\\_block.pdf](http://www.xilinx.com/support/documentation/ip_documentation/bram_block.pdf)

- Microprocessor Debug Module – DS641

[http://www.xilinx.com/support/documentation/ip\\_documentation/mdm.pdf](http://www.xilinx.com/support/documentation/ip_documentation/mdm.pdf)

- LMB Block RAM Interface Controller – DS452

[http://www.xilinx.com/support/documentation/ip\\_documentation/lmb\\_bram\\_if\\_cntlr.pdf](http://www.xilinx.com/support/documentation/ip_documentation/lmb_bram_if_cntlr.pdf)

# Documentation

## ▪ IP

- JTAGPPC Controller – DS298

[http://www.xilinx.com/support/documentation/ip\\_documentation/jtagppc\\_cntlr.pdf](http://www.xilinx.com/support/documentation/ip_documentation/jtagppc_cntlr.pdf)

- Processor System Reset Module – DS402

[http://www.xilinx.com/support/documentation/ip\\_documentation/proc\\_sys\\_reset.pdf](http://www.xilinx.com/support/documentation/ip_documentation/proc_sys_reset.pdf)

- Clock Generator v2.0 – DS614

[http://www.xilinx.com/support/documentation/ip\\_documentation/clock\\_generator.pdf](http://www.xilinx.com/support/documentation/ip_documentation/clock_generator.pdf)

# Documentation

- IP

- Utility Vector Logic – DS481

[http://www.xilinx.com/support/documentation/ip\\_documentation/util\\_vector\\_logic.pdf](http://www.xilinx.com/support/documentation/ip_documentation/util_vector_logic.pdf)

- Utility IO Multiplexer – DS694

[http://www.xilinx.com/support/documentation/ip\\_documentation/util\\_io\\_mux.pdf](http://www.xilinx.com/support/documentation/ip_documentation/util_io_mux.pdf)

# Documentation

## ▪ ML505/506/507

- ML505 Overview

<http://www.xilinx.com/ml505>

- ML506 Overview

<http://www.xilinx.com/ml506>

- ML507 Overview

<http://www.xilinx.com/ml507>

- ML505/506/507 Evaluation Platform User Guide – UG347

[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug347.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug347.pdf)

- ML505/506/507 Getting Started Tutorial – UG348

[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug348.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug348.pdf)

- ML505/506/507 Reference Design User Guide – UG349

[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug349.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug349.pdf)

# Documentation

- **ML505/506/507**

- ML505/506/507 Schematics

[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ml50x\\_schematics.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ml50x_schematics.pdf)

- ML505/506/507 Bill of Material

[http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ml505\\_501\\_bom.xls](http://www.xilinx.com/support/documentation/boards_and_kits/ml505_501_bom.xls)