



ML510 Two GTXs IBERT Design Creation Using 10.1i SP3 ChipScope™ Pro

September 2008



ML510 IBERT Overview

- Software Requirements
- Design Generation
 - Highlighting the Virtex-5 RocketIO™ GTX Transceivers

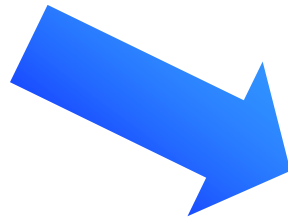
Additional Setup Details

- Refer to ml510_overview_setup.ppt for details on:
 - Software Requirements
 - ML510 Board Setup
 - **Equipment and Cables**
 - **Software**
 - **Network**
 - Terminal Programs
 - **This presentation requires the 9600-8-N-1 Baud terminal setup**



ISE Software Requirement

- Xilinx ISE 10.1i SP3 software




ChipScope Software Requirement

- Xilinx ChipScope Pro 10.1i SP3



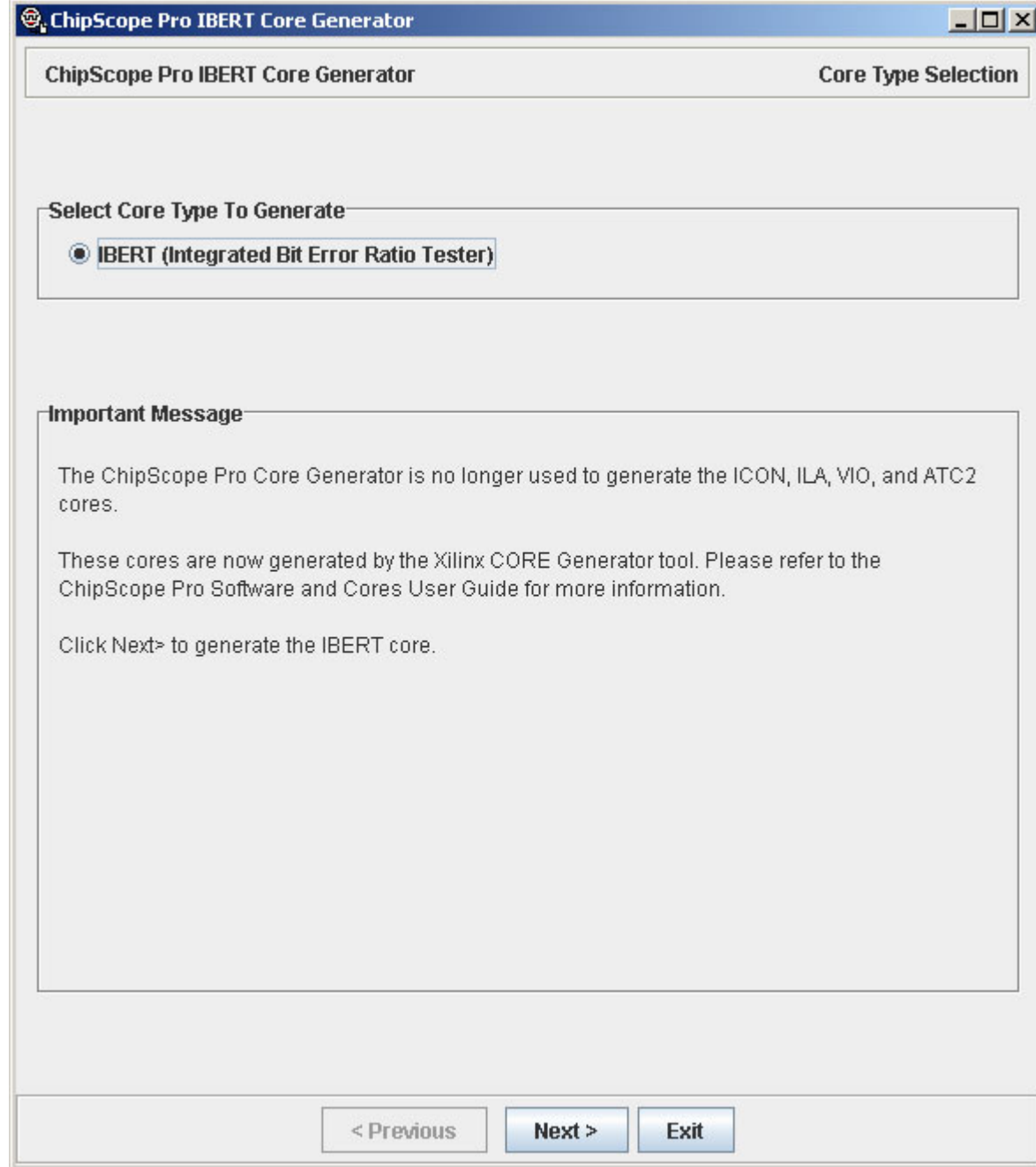
ChipScope Pro Analyzer

Release Version: 10.1 03
Application Version: K.39 (Build 10103.8.234.834)
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IBERT Generation

- Open the ChipScope Pro IBERT Core Generator



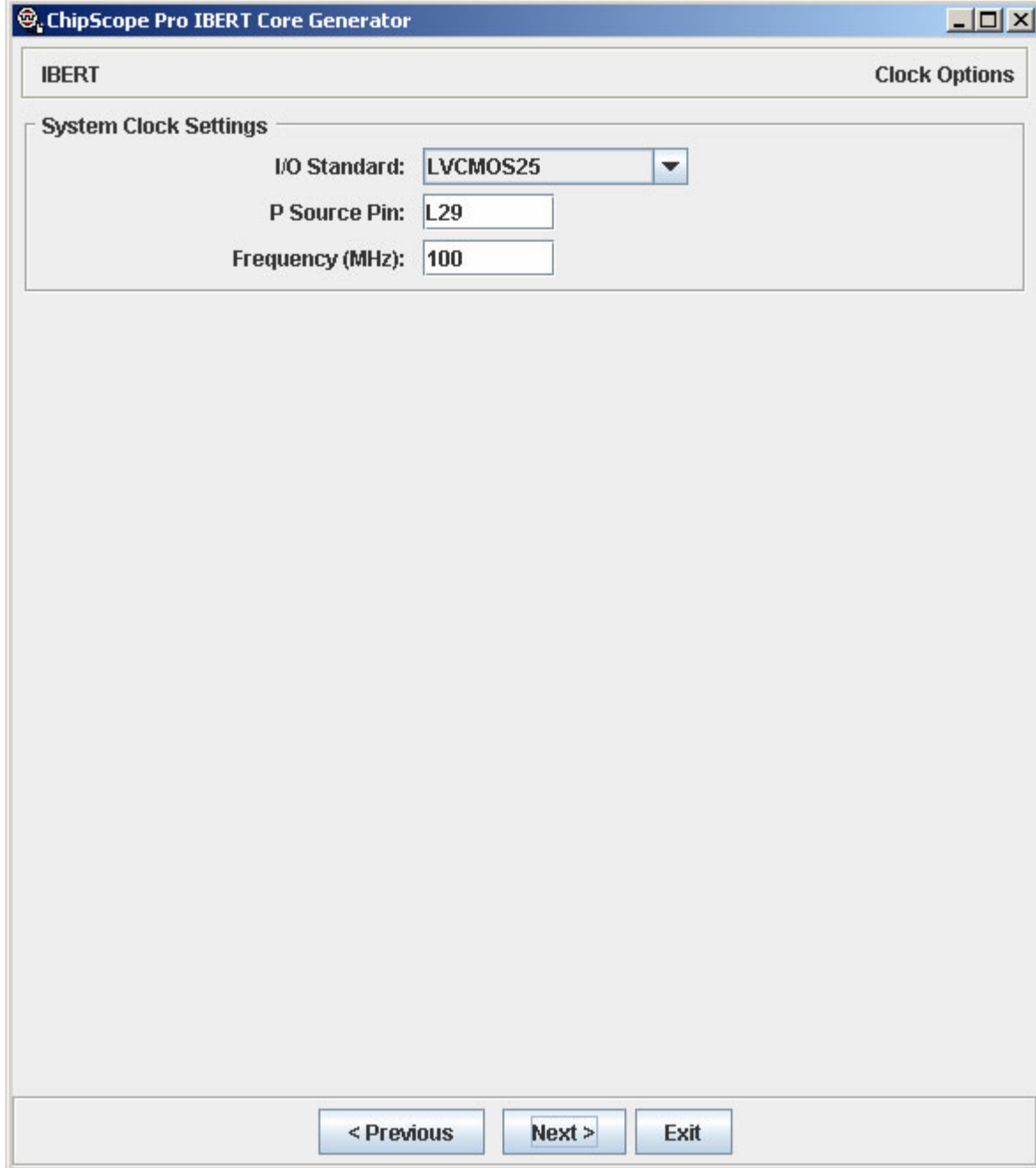
IBERT Generation

- Set the output to your design directory
- Make these settings:
 - Virtex5
 - xc5vfx130t
 - ff1738
 - -2

The screenshot shows the 'ChipScope Pro IBERT Core Generator' window. The title bar includes the application name and standard window controls. The main window is titled 'IBERT' and has a 'General Options' tab selected. It is divided into several sections: 'Design Files' with an 'Output Bitstream' field containing 'C:\ml510_ibert_2gbs\ml510_ibert_design.bit' and a 'Browse' button; 'Device Selection' with four dropdown menus for 'Device Family' (Virtex5), 'Device' (xc5vfx130t), 'Package' (ff1738), and 'Speed Grade' (-2); and 'Silicon Revision' with a dropdown menu set to 'Production'. At the bottom, there are three buttons: '< Previous', 'Next >', and 'Exit'.

IBERT Generation

- System Clock Settings:
 - I/O Std: LVCMOS25
 - P Source Pin: L29
 - Set Freq: 100



The screenshot shows the 'ChipScope Pro IBERT Core Generator' window. The title bar includes the application name and standard window controls. The main window has a tab labeled 'IBERT' and a 'Clock Options' button in the top right corner. Below the tab is a section titled 'System Clock Settings' which contains three configuration fields: 'I/O Standard' is a dropdown menu set to 'LVCMOS25', 'P Source Pin' is a text input field containing 'L29', and 'Frequency (MHz)' is a text input field containing '100'. At the bottom of the window, there are three buttons: '< Previous', 'Next >', and 'Exit'.

IBERT Generation

- Set the Pattern Settings as shown

The screenshot shows the 'ChipScope Pro IBERT Core Generator' window. The title bar includes the application name and standard window controls. The main window is divided into several sections:

- IBERT** (top left) and **MGT Options** (top right).
- Resource Usage**: Number of GTX Duals used: 0 out of 10; Number of DCMs used: 0 out of 12.
- Pattern Settings**: A list of checkboxes for different PRBS patterns, all of which are checked. A red box highlights the first seven options: PRBS 7-bit, PRBS 7-bit Alt, PRBS 9-bit, PRBS 11-bit, PRBS 15-bit, PRBS 20-bit, and PRBS 23-bit. Other checked options include PRBS 29-bit, PRBS 31-bit, User Pattern, Framed Counter, and Idle Pattern.
- GTX Settings**: Two sections for configuring GTX Duals. The first section is for 'Enable GTX_DUAL_X0Y0 (MGT130)' with Ref Clock Pins (P, N) set to AW9, AY9. It lists TX Pins (P, N) and RX Pins (P, N) for GTX 0 and GTX 1. The second section is for 'Enable GTX_DUAL_X0Y1 (MGT126)' with Ref Clock Pins (P, N) set to AW4, AY4, and lists TX and RX pins for GTX 0 and GTX 1. Both sections have 'Frequency Mode' set to 'Invalid Line Rate' and empty text boxes for 'Max Line Rate (Mbps)' and 'Ref Clock Freq (MHz)'.

At the bottom of the window are three buttons: '< Previous', 'Next >', and 'Exit'.

IBERT Generation

- Select Enable GTX_DUAL_X0Y7
 - Set Max Line Rate to 3000
 - Set Ref Clock Frequency to 150
- Select Enable GTX_DUAL_X0Y8
 - Set Max Line Rate to 2500
 - Set Ref Clock Frequency to 125

The screenshot shows the 'ChipScope Pro IBERT Core Generator' window. The title bar reads 'ChipScope Pro IBERT Core Generator'. The main window is titled 'IBERT' and has a 'MGT Options' button in the top right corner. Below the title bar, there is a 'Resource Usage' section showing 'Number of GTX Duals used: 2 out of 10' and 'Number of DCMs used: 6 out of 12'. The interface is divided into two main panels: 'Pattern Settings' on the left and 'GTX Settings' on the right. The 'Pattern Settings' panel contains a list of checkboxes, all of which are checked: PRBS 7-bit, PRBS 7-bit Alt, PRBS 9-bit, PRBS 11-bit, PRBS 15-bit, PRBS 20-bit, PRBS 23-bit, PRBS 29-bit, PRBS 31-bit, User Pattern, Framed Counter, and Idle Pattern. The 'GTX Settings' panel is divided into two sections, one for GTX_DUAL_X0Y7 (MGT120) and one for GTX_DUAL_X0Y8 (MGT124). Each section has a checked 'Enable' checkbox, a 'Ref Clock Pins (P, N)' field, a table for TX and RX pins, 'Frequency Mode' (set to High Freq), 'Max Line Rate (Mbps)' (3000 for GTX0Y7, 2500 for GTX0Y8), and 'Ref Clock Freq (MHz)' (150.000 for GTX0Y7, 125.000 for GTX0Y8). At the bottom of the window, there are three buttons: '< Previous', 'Next >', and 'Exit'.

IBERT MGT Options

Resource Usage
Number of GTX Duals used: 2 out of 10 Number of DCMs used: 6 out of 12

Pattern Settings

- PRBS 7-bit
- PRBS 7-bit Alt
- PRBS 9-bit
- PRBS 11-bit
- PRBS 15-bit
- PRBS 20-bit
- PRBS 23-bit
- PRBS 29-bit
- PRBS 31-bit
- User Pattern
- Framed Counter
- Idle Pattern

GTX Settings

Enable GTX_DUAL_X0Y7 (MGT120)

Ref Clock Pins (P, N): F4, F3

	TX Pins (P, N)	RX Pins (P, N)
GTX 0:	D2, E2	E1, F1
GTX 1:	J2, H2	H1, G1

Frequency Mode: High Freq (2400Mbps - 6500Mbps)

Max Line Rate (Mbps): 3000

Ref Clock Freq (MHz): 150.000 (FB=4, REF=1, DIVSEL=2)

Enable GTX_DUAL_X0Y8 (MGT124)

Ref Clock Pins (P, N): C4, C3

	TX Pins (P, N)	RX Pins (P, N)
GTX 0:	B6, B5	A5, A4
GTX 1:	B1, B2	A2, A3

Frequency Mode: High Freq (2400Mbps - 6500Mbps)

Max Line Rate (Mbps): 2500

Ref Clock Freq (MHz): 125.000 (FB=4, REF=1, DIVSEL=2)

< Previous Next > Exit

IBERT Generation

- Leave this screen as is



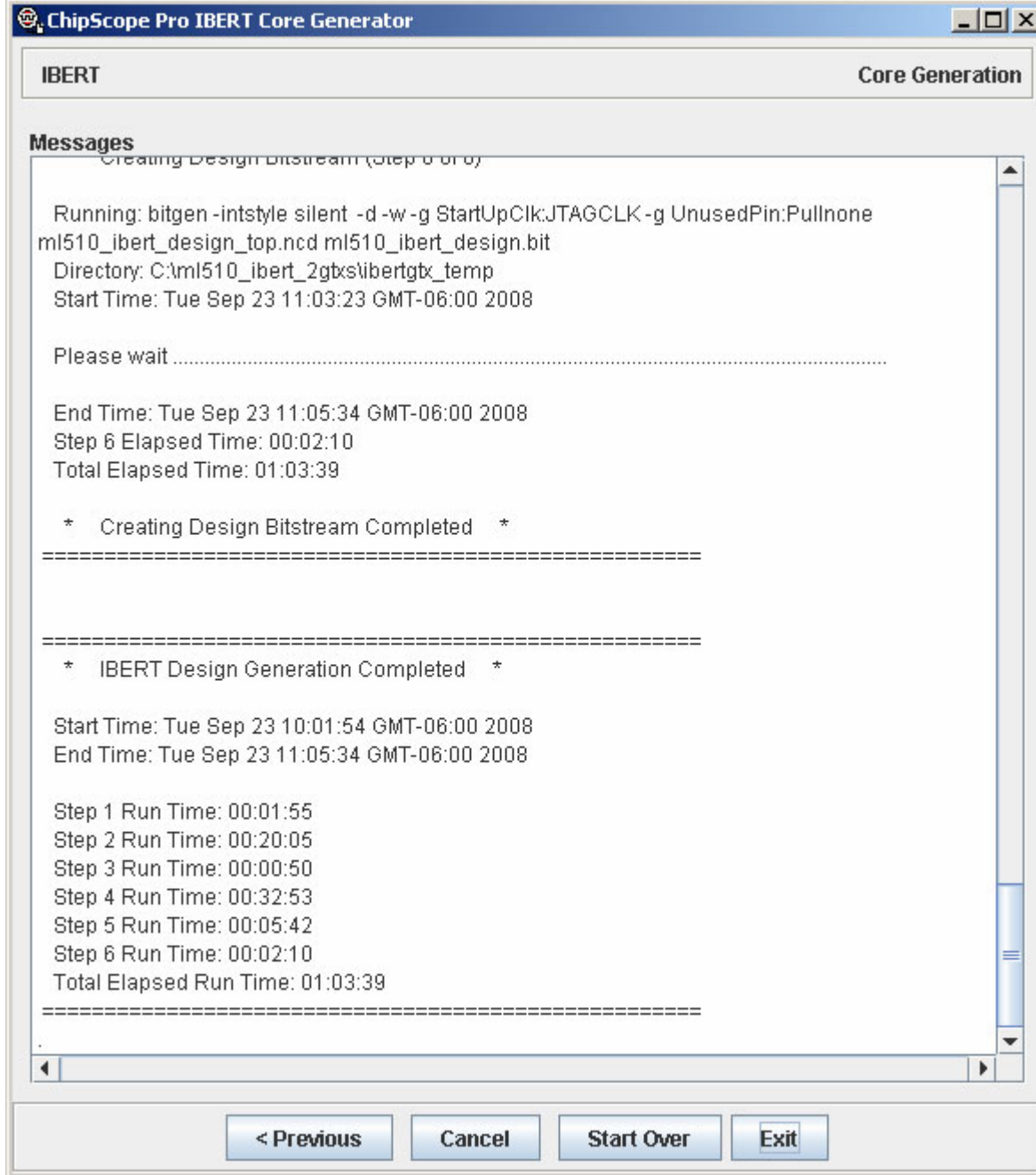
IBERT Generation

- Click Generate Design



IBERT Generation

- Bitstream is compiled and ready to use



Other GTXs

- Other GTXs can be selected and implemented:
 - GTX_DUAL_X0Y0 = MGT130 = PCIe Slot A
 - GTX_DUAL_X0Y1 = MGT126 = PCIe Slot A
 - GTX_DUAL_X0Y2 = MGT122 = PCIe Slot A
 - GTX_DUAL_X0Y3 = MGT118 = PM
 - GTX_DUAL_X0Y4 = MGT114 = PM
 - GTX_DUAL_X0Y5 = MGT112 = PM
 - GTX_DUAL_X0Y6 = MGT116 = PM
 - GTX_DUAL_X0Y9 = MGT128 = PCIe Slot B

Documentation

- Virtex-5
 - Silicon Devices
http://www.xilinx.com/products/silicon_solutions
 - Virtex-5 Multi-Platform FPGA
http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5
 - Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms
http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
 - Virtex-5 FPGA DC and Switching Characteristics Data Sheet
http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf

Documentation

- Virtex-5
 - Virtex-5 FPGA User Guide
http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
 - Virtex-5 FPGA Configuration User Guide
http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
 - Virtex-5 System Monitor User Guide
http://www.xilinx.com/support/documentation/user_guides/ug192.pdf
 - Virtex-5 Packaging and Pinout Specification
http://www.xilinx.com/support/documentation/user_guides/ug195.pdf

Documentation

- Virtex-5 RocketIO

- RocketIO GTP Transceivers

http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTP.htm

- RocketIO GTX Transceivers

http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTX.htm

- RocketIO GTP Transceiver User Guide – UG196

http://www.xilinx.com/support/documentation/user_guides/ug196.pdf

- RocketIO GTX Transceiver User Guide – UG198

http://www.xilinx.com/support/documentation/user_guides/ug198.pdf

Documentation

- Design Resources

- ISE Development Tools and IP

<http://www.xilinx.com/ise>

- Integrated Software Environment (ISE) Foundation Resources

http://www.xilinx.com/ise/logic_design_prod/foundation.htm

- ISE Manuals

http://www.xilinx.com/support/software_manuals.htm

- ISE Development System Reference Guide

<http://toolbox.xilinx.com/docsan/xilinx10/books/docs/dev/dev.pdf>

- ISE Development System Libraries Guide

http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5_hdl/virtex5_hdl.pdf

Documentation

- Additional Design Resources
 - Customer Support
<http://www.xilinx.com/support>
 - Xilinx Design Services:
<http://www.xilinx.com/xds>
 - Titanium Dedicated Engineering:
<http://www.xilinx.com/titanium>
 - Education Services:
<http://www.xilinx.com/education>
 - Xilinx On Board (Board and kit locator):
<http://www.xilinx.com/xob>

Documentation

- Platform Studio

- Embedded Development Kit (EDK) Resources

<http://www.xilinx.com/edk>

- Embedded System Tools Reference Manual

http://www.xilinx.com/support/documentation/sw_manuels/edk10_est_rm.pdf

- EDK Concepts, Tools, and Techniques

http://www.xilinx.com/support/documentation/sw_manuels/edk_ctt.pdf

Documentation

- PowerPC 440
 - PowerPC 440 Processor
<http://www.xilinx.com/powerpc>
 - Embedded Processor Block in Virtex-5 FPGAs Reference Guide – UG200
http://www.xilinx.com/support/documentation/user_guides/ug200.pdf
 - PPC440 Virtex-5 Wrapper – DS621
http://www.xilinx.com/support/documentation/ip_documentation/ppc440_virtex5.pdf
 - DDR2 Memory Controller for PowerPC 440 Processors – DS567
http://www.xilinx.com/support/documentation/data_sheets/ds567.pdf

Documentation

- MicroBlaze
 - MicroBlaze Processor
<http://www.xilinx.com/microblaze>
 - MicroBlaze Processor Reference Guide – UG081
http://www.xilinx.com/support/documentation/sw_manuals/mb_ref_guide.pdf

Documentation

- Memory Solutions

- Demos on Demand – Memory Interface Solutions with Xilinx FPGAs

http://www.demosondemand.com/clients/xilinx/001/page_new2/index.asp#35

- Xilinx Memory Corner

http://www.xilinx.com/products/design_resources/mem_corner

- Additional Memory Resources

<http://www.xilinx.com/support/software/memory/protected/index.htm>

- Xilinx Memory Interface Generator (MIG) 2.2 User Guide

http://www.xilinx.com/support/documentation/ip_documentation/ug086.pdf

- Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator

http://www.xilinx.com/support/documentation/white_papers/wp260.pdf

Documentation

- ChipScope Pro
 - ChipScope Pro 10.1i Serial IO Toolkit User Manual
http://www.xilinx.com/ise/verification/chipscope_pro_siotk_10_1_ug213.pdf
 - ChipScope Pro 10.1i ChipScope Pro Software and Cores User Guide
http://www.xilinx.com/ise/verification/chipscope_pro_sw_cores_10_1_ug029.pdf

Documentation

- Ethernet
 - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet
http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_ds550.pdf
 - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide
http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_gsg340.pdf
 - Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide
http://www.xilinx.com/support/documentation/user_guides/ug194.pdf
 - LightWeight IP (lwIP) Application Examples – XAPP1026
http://www.xilinx.com/support/documentation/application_notes/xapp1026.pdf

Documentation

- PLB v4.6 IP
 - Processor Local Bus (PLB) v4.6 Data Sheet – DS531
http://www.xilinx.com/support/documentation/ip_documentation/plb_v46.pdf
 - Multi-Port Memory Controller (MPMC) – DS643
http://www.xilinx.com/support/documentation/ip_documentation/mpmc.pdf
 - XPS Multi-Channel External Memory Controller (XPS MCH EMC) – DS575
http://www.xilinx.com/support/documentation/ip_documentation/xps_mch_emc.pdf
 - XPS LocalLink TEMAC – DS537
http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_temac.pdf
 - XPS LocalLink FIFO – DS568
http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_fifo.pdf

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- PLB v4.6 IP
 - XPS IIC Bus Interface – DS606
http://www.xilinx.com/support/documentation/ip_documentation/xps_iic.pdf
 - XPS SYSACE (System ACE) Interface Controller – DS583
http://www.xilinx.com/support/documentation/ip_documentation/xps_sysace.pdf
 - XPS Timer/Counter – DS573
http://www.xilinx.com/support/documentation/ip_documentation/xps_timer.pdf
 - XPS Interrupt Controller – DS572
http://www.xilinx.com/support/documentation/ip_documentation/xps_intc.pdf
 - Using and Creating Interrupt-Based Systems Application Note
http://www.xilinx.com/support/documentation/application_notes/xapp778.pdf

Documentation

- PLB v4.6 IP
 - XPS General Purpose Input/Output (GPIO) – DS569
http://www.xilinx.com/support/documentation/ip_documentation/xps_gpio.pdf
 - XPS External Peripheral Controller (EPC) – DS581
http://www.xilinx.com/support/documentation/ip_documentation/xps_epc.pdf
 - XPS 16550 UART – DS577
http://www.xilinx.com/support/documentation/ip_documentation/xps_uart16550.pdf
 - PLBV46 to DCR Bridge Data Sheet – DS578
http://www.xilinx.com/support/documentation/ip_documentation/plbv46_dcr_bridge.pdf

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- IP
 - Local Memory Bus Data Sheet – DS445
http://www.xilinx.com/support/documentation/ip_documentation/lmb_v10.pdf
 - Block RAM Block Data Sheet – DS444
http://www.xilinx.com/support/documentation/ip_documentation/bram_block.pdf
 - Microprocessor Debug Module Data Sheet – DS641
http://www.xilinx.com/support/documentation/ip_documentation/mdm.pdf
 - LMB Block RAM Interface Controller Data Sheet – DS452
http://www.xilinx.com/support/documentation/ip_documentation/lmb_bram_if_cntlr.pdf
 - Device Control Register Bus (DCR) v2.9 Data Sheet – DS406
http://www.xilinx.com/support/documentation/ip_documentation/dcr_v29.pdf

Documentation

- IP
 - JTAGPPC Controller Data Sheet – DS298
http://www.xilinx.com/support/documentation/ip_documentation/jtagppc_cntlr.pdf
 - Processor System Reset Module Data Sheet – DS402
http://www.xilinx.com/support/documentation/ip_documentation/proc_sys_reset.pdf
 - Clock Generator v2.0 Data Sheet – DS614
http://www.xilinx.com/support/documentation/ip_documentation/clock_generator.pdf
 - Util Bus Split Operation Data Sheet – DS484
http://www.xilinx.com/support/documentation/ip_documentation/util_bus_split.pdf

Documentation

- ML510
 - ML510 Overview
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 - ML510 Evaluation Platform User Guide – UG356
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 - ML510 Reference Design User Guide – UG355
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 - ML510 Quickstart Tutorial
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Documentation

- ML510

- ML510 Schematics

- http://www.xilinx.com/support/documentation/boards_and_kits/ml510_schematics.pdf

- ML510 Bill of Material

- http://www.xilinx.com/support/documentation/boards_and_kits/ml510_bom.xls