Digital Core Design
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Features
• Available under terms of the SignOnce IP License
• Full IEEE-754 compliance
• Single precision real format support
• Simple interface
• No programming required
• 21 levels pipeline
• Full accuracy and precision
• Results available at every clock
• Overflow, underflow and invalid operation flags
• Fully configurable
• Fully synthesizable, static synchronous design with no internal tri-states

Table 1: Example Implementation Statistics

<table>
<thead>
<tr>
<th>Family</th>
<th>Example Device</th>
<th>Fmax (MHz)</th>
<th>Slices</th>
<th>IOB</th>
<th>GCLK</th>
<th>BRAM</th>
<th>MULT/ DSP48</th>
<th>DCM</th>
<th>MGT</th>
<th>PPC</th>
<th>Design Tools</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spartan-3™</td>
<td>XC3S400-5</td>
<td>81</td>
<td>1728</td>
<td>102</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>N/A</td>
<td>ISE 7.1.03i</td>
</tr>
<tr>
<td>Spartan-3E™</td>
<td>XC3ES500-4</td>
<td>64</td>
<td>1728</td>
<td>102</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>N/A</td>
<td>N/A</td>
<td>ISE 7.1.03i</td>
</tr>
<tr>
<td>Virtex-II Pro™</td>
<td>XC2VP4-7</td>
<td>134</td>
<td>1728</td>
<td>102</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ISE 7.1.03i</td>
</tr>
<tr>
<td>Virtex-4™</td>
<td>XC4VFX12-12</td>
<td>166</td>
<td>1728</td>
<td>102</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ISE 7.1.03i</td>
</tr>
</tbody>
</table>

Notes:
1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
2) Assuming all core I/Os and clocks are routed off-chip
Applications

Paragraph or bullet listing of potential systems that might use this core.

General Description

The DFPDIV uses the pipelined mathematics algorithm to divide two arguments. The input numbers format is according to IEEE-754 standard. DFPDIV supports the single precision real numbers. Divide operation was pipelined up to 21 levels. Input data are fed every clock cycle. The first result appears after latency depending on pipeline level and next results are available each clock cycle. Full IEEE-754 precision and accuracy were included.

Functional Description

The DFPDIV Core is partitioned on the functionally independent blocks as shown in Figure 1. The blocks functionality is described below.

Arguments Checker
Performs input data analyze against IEEE-754 number standard compliance. The appropriate numbers and information about the input data classes are given as the results to Main FP Pipelined Unit.

Main FP Pipelined Unit
Performs floating point divide function. Gives the complex information about the results and makes final flags settings.

Result Composer
Performs result rounding function, data alignment to IEEE-754 standard, and the final flags setting.

Core Modifications

DFPDIV can be fully customized accordingly to customer needs.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.
Table 2: Core I/O Signals.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>Input</td>
<td>Global system clock</td>
</tr>
<tr>
<td>rst</td>
<td>Input</td>
<td>Global system reset</td>
</tr>
<tr>
<td>en</td>
<td>Input</td>
<td>Enable computing</td>
</tr>
<tr>
<td>adatai[31:0]</td>
<td>Input</td>
<td>A data bus input</td>
</tr>
<tr>
<td>bdatai[31:0]</td>
<td>Input</td>
<td>B data bus input</td>
</tr>
<tr>
<td>datao[31:0]</td>
<td>Output</td>
<td>Data bus output</td>
</tr>
<tr>
<td>ofo</td>
<td>Output</td>
<td>Overflow flag</td>
</tr>
<tr>
<td>ufo</td>
<td>Output</td>
<td>Underflow flag</td>
</tr>
<tr>
<td>ifo</td>
<td>Output</td>
<td>Invalid result flag</td>
</tr>
</tbody>
</table>

Verification Methods

The DFPDIV has been verified in simulation using fully automated testbench that includes several test programs. The reference responses have been captured from an original IEEE-754 compliant coprocessor chip. This testbench and set of tests are included in the HDL source package as a standard option.

The DFPDIV has also been verified using DCD testing board. The several division set of tests were automatically compared to the reference results computed by PC coprocessor.

Recommended Design Experience

The users should be familiar with the floating point systems and skilled in any programming language.

Ordering Information

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