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Features
• Available under terms of the SignOnce IP License
• Supports Virtex™, Virtex-II, Spartan™-II, and Spartan-IIE devices
• Parallel Distributed Arithmetic (PDA) architecture
• Input data word: 16 bits
• Coefficient data width: 24 bits
• Output data word: 24 bits
• Signed arithmetic
• Internal cascading for better performance
• Works on both symmetrical and asymmetrical coefficients

Applications
• Filter applications
  - High-pass
  - Low-pass
  - Band-pass
  - rcosine & root rcosine filter
• Speech synthesis
• Waveform shaping

AllianceCORE™ Facts

<table>
<thead>
<tr>
<th>Core Specifics</th>
<th>Provided with Core</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design File Formats</td>
<td>EDIF netlist, .ndg, Verilog RTL</td>
</tr>
<tr>
<td>Constraints Files</td>
<td>tap8virt.ucf, tap8virt.pcf, tap8sp.ucf, tap8sp.pcf</td>
</tr>
<tr>
<td>Verification Tool</td>
<td>Testbench, test vectors, reference module, matlab files, sdf file, Assembly Program</td>
</tr>
<tr>
<td>Instantiation Templates</td>
<td>Verilog</td>
</tr>
<tr>
<td>Reference designs &amp; application notes</td>
<td>None</td>
</tr>
<tr>
<td>Additional Items</td>
<td>Hardware demo board of Xilinx, 89C52 hardware interface for physical verification</td>
</tr>
<tr>
<td>Tools Used</td>
<td>ModelSim, Xilinx Foundation 3.1</td>
</tr>
<tr>
<td>Support</td>
<td>Support provided by eInfochips, Inc.</td>
</tr>
</tbody>
</table>

Digital decimation in DSL applications
High speed modems
  - ADSL
  - VDSL
  - SDSL
Image processing
Digital demodulator
  - HDTV
  - DTV

Table 1: 8-Tab, Nonsymmetrical Example of Implementation Statistics

<table>
<thead>
<tr>
<th>Supported Family</th>
<th>Device Tested</th>
<th>Slices</th>
<th>Clock IOBs</th>
<th>IOBs</th>
<th>Performance (MHz)</th>
<th>Xilinx Tools</th>
<th>Special Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex</td>
<td>XCV400-4</td>
<td>694</td>
<td>1</td>
<td>42</td>
<td>66</td>
<td>M3.1i</td>
<td>N/A</td>
</tr>
<tr>
<td>Virtex-II</td>
<td>XC2V250-5</td>
<td>693</td>
<td>1</td>
<td>42</td>
<td>90(^1)</td>
<td>M3.3i</td>
<td>N/A</td>
</tr>
<tr>
<td>Spartan-II</td>
<td>XC2S100-6</td>
<td>693</td>
<td>1</td>
<td>42</td>
<td>78</td>
<td>M3.1i</td>
<td>Works at 91 MHz in post-synthesis simulation</td>
</tr>
<tr>
<td>Spartan-IIE</td>
<td>XC2S200E-6</td>
<td>823</td>
<td>1</td>
<td>42</td>
<td>83(^1)</td>
<td>WebPack ISE 4.1</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Notes:
1. Based on constraints
**General Description**

FIR filters are basic building blocks used in digital signal processing, taxing the performance that DSP hardware can deliver.

Multiply accumulates must be performed at an ever-increasing rate and demands in the billions of MACs-per-second range are now common.

Field programmable gate arrays (FPGAs) using distributed arithmetic algorithms can implement large numbers of taps at MHz data sample rates, outperforming DSP processors by one or two orders of magnitude.

Sample rates can be handled efficiently over a wide range by applying the proper structure that just meets the required performance with the least number of FPGA configurable logic blocks (CLBs).

**Functional Description**

Data presented at the filter \( x_i \) data port is stored within the filter module in an array of internal registers, one per tap.

Filter coefficients provided by the user are stored in internal look-up tables and accessed during filter operation in accordance with the parallel-distributed arithmetic algorithm.

Partial results from each look-up table are summed to form a final result at the filter output port \( x_o \). Given information about the bit-width of the input data, coefficients, and the number of filter taps, the parameterization window indicates the number of bits necessary at the output port to encompass the dynamic range of the filter output.

The output port may be truncated to fewer bits if desired. Truncation occurs by trimming as many LSBs from the result as necessary to deliver the requested number of bits at the output port. Truncation does not significantly reduce the amount of logic required by the filter since, internally, full precision is always maintained.

The filter accepts a new input data word and produces a new filtered result on every clock cycle.
Pinout

Pinout signals are illustrated in Figure 2 and described in Table 2.

Table 2: Core Signal Pinout

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>xi_data[n:0]</td>
<td>Input</td>
<td>Parallel data input</td>
</tr>
<tr>
<td>xi_clk</td>
<td>Input</td>
<td>Input data is captured and output data is formed on every rising edge of xi_clk.</td>
</tr>
<tr>
<td>xi_reset_h</td>
<td>Input</td>
<td>For initialization</td>
</tr>
<tr>
<td>xo_data</td>
<td>Output</td>
<td>Filter result: parallel data out</td>
</tr>
<tr>
<td>xo_clk</td>
<td>Output</td>
<td>Output clock</td>
</tr>
</tbody>
</table>

Internal Cascading of Multiple PDA FIR Filter

Internal cascading of multiple PDA FIR Filters is used to gain slice and speed made available by the FPGA architecture.

Verification Methods

The core has been verified using in-house-generated test vectors and using Modelsim, Matlab, and an assembly program written for the 89c52 controller on an xc4000hq240-4 (Virtex) device and an xc2s100-6-tq144 (Spartan-II) device. The core has not been verified on an xc2v250-5-cs144 (Virtex-II) device or an xc2s200e-pq208-6 (Spartan-IIIE) device.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This AllianceCORE product is available from Xilinx AllianceCORE partner, eInfochips, Inc., under terms of the SignOnce IP License. To learn about the SignOnce IP License program, contact eInfochips, Inc., visit www.xilinx.com/ipcenter/signonce.htm, or write to commonlicense@xilinx.com.

Please contact eInfochips, Inc., for pricing and additional information about this AllianceCORE product.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For AllianceCORE-specific information:


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