



FAQ110 (v1.0) December 2, 2002

Spartan-IIE Family Extension: Frequently Asked Questions

1. What is the Spartan-IIE Family Extension?

The Spartan™-IIE extension is the addition of two new higher density devices to the already successful Spartan-IIE product family. The addition of the two higher densities will help designers address designs which require larger gate counts and more I/O pins. Another benefit from the extension is the large increase in RAM (both Block and Distributed) found in the two largest devices.

2. How will the new devices help you as a designer?

Companies making cost-sensitive products such as plasma displays, set-top-boxes, and broadcast video equipment require fast time-to-market in order to deliver the best products to market, but are also extremely cost sensitive. The expanded Spartan-IIE family delivers increased I/O count and density to allow you to use Spartan-IIE FPGAs in your more advanced products while achieving your system cost goals.

These benefits include:

- **Lowest cost per I/O** — You get more I/O at much lower prices than any competing FPGA
- **Up to 514 I/O** — The maximum I/O availability in the industry allows you to put higher density ASICs into FPGAs and stay with the benefits of FPGA technology in larger designs
- **Supports 19 standards, including LVDS, HSTL, and PCI** — This gives you the maximum flexibility available in the industry in IO implementation. Thus you can easily bridge your design to numerous I/O standards on the same board
- **Four DLLs** — The only FPGA to support DLLs with the largest number of functionality in the low-cost FPGA marketplace. The DLLs will allow for easy clock duplication, quick frequency adjustment, faster state machines using different clock phases, de-skew the incoming clock, and generate fast setup and hold times or fast clock to outs
- **Over one billion MACs/sec per dollar** — Implement high performance DSP functionality and replace DSP functions at lowest cost possible
- **Extensive IP core support** — You can get PCI, extensive DSP cores, and

many other predesigned and tested solutions to increase your productivity and decrease design time

3. What are the I/O advantages associated Spartan-IIe FPGAs?

Spartan-IIe devices have up to 514 I/O with up to 100% more I/Os than any other competing FPGA solution in the same density range. For instance the XC2S600E has 200 more I/O than the largest competing low cost FPGA. The Spartan-IIe devices support the largest number of I/O standards in the low cost FPGA market and also have the lowest cost per pin available from any FPGA supplier. Designers can now take advantage of the greater number of I/O pins, combined with the advantages of reprogrammability to replace designs typically done with ASICs.

4. How long has Xilinx been delivering low cost FPGAs?

Since introducing Spartan more than four years ago, Xilinx has delivered four generations of these devices, offering customers a low cost, programmable alternative to ASICs without NRE costs. In 2003, the company is on track to deliver a fifth generation of the Spartan Series, reaching even higher densities at significantly lower price points.

In September 2002 we announced delivery of over 40 million Spartan series devices into the hands of customers. Starting as low as \$2.55 per device, the Spartan series is the lowest-cost family of FPGAs shipping today. A cornerstone of the company's market diversification strategy, Spartan represents over 13 percent of Xilinx revenue.

5. What devices have been added to the Spartan-IIe family?

XC2S400E and XC2S600E are new members of Spartan-IIe family:

Table 1: Spartan-IIe FPGA Family Members

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O ⁽¹⁾	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	265	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

6. Will there be new packages available for the higher pin count devices?

In addition to the existing FT256 and FG456 packages available in the existing family, the FG676 will be added for the 400K and 600K gate devices.

Table 2: Spartan-IIE User I/O Chart

Device	Maximum User I/O	Available User I/O According to Package Type				
		TQ144	PQ208	FT256	FG456	FG676
XC2S50E	182	102	146	182	-	-
XC2S100E	202	102	146	182	202	-
XC2S150E	265	-	146	182	265	-
XC2S200E	289	-	146	182	289	-
XC2S300E	329	-	146	182	329	-
XC2S400E	410	-	-	182	329	410
XC2S600E	514	-	-	-	329	514

Notes:

1. User I/O counts include the four global clock/user input pins.

2. Will density migration be available?

Yes. Following the tradition of Xilinx FPGA families, the Spartan-IIE family will continue to support density migration across common packages without changing the PC board footprint. For example, when using an FG456 package, six density members of the Spartan-IIE family can be implemented, providing outstanding flexibility for design revision, upgrade, or cost optimization.

Table 3: Standards Supported by I/O (Typical Values)

Device Family	I/O Standards												Differential Signaling				
	LVTTTL	LVCMOS	PCI33	PCI66	GTL	GTL+	SSTL		AGP	HSTL			CTT	LVDS			LVPECL
							2	3		2X	I	III		IV	Clock	Data	
Spartan-IIE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

3. What speed and temperature grades will be available for the new devices?

The family extension will be available in three temperature ranges, “C”, “I” and “Q” as shown in the chart below. The -6 and -7 speed grades will be available in the entire family including the two new densities (Table 4).

C = commercial: 0°C to +85°C

I = industrial: -40°C to +100°C

Q = Automotive: -40°C to +125°C

Table 4: Spartan-IIE Package and Speed Grade Availability

Device	Pins	144	208	256	456	676
	Type	Plastic TQFP	Plastic PQFP	Fine Pitch BGA	Fine Pitch BGA	Fine Pitch BGA
	Code	TQ144	PQ208	FT256	FG456	FG676
XC2S50E	-6	C, I, Q	C, I, Q	C, I, Q	-	-
	-7	C	C	C	-	-

Table 4: Spartan-IIE Package and Speed Grade Availability (Continued)

Device	Pins	144	208	256	456	676
	Type	Plastic TQFP	Plastic PQFP	Fine Pitch BGA	Fine Pitch BGA	Fine Pitch BGA
	Code	TQ144	PQ208	FT256	FG456	FG676
XC2S100E	-6	C, I, Q	C, I, Q	C, I, Q	C, I, Q	-
	-7	C	C	C	C	-
XC2S150E	-6	-	C, I, Q	C, I, Q	C, I, Q	-
	-7	-	C	C	C	-
XC2S200E	-6	-	C, I, Q	C, I, Q	C, I, Q	-
	-7	-	C	C	C	-
XC2S300E	-6	-	C, I, Q	C, I, Q	C, I, Q	-
	-7	-	C	C	C	-
XC2S400E	-6	-	-	C, I, Q	C, I, Q	C, I
	-7	-	-	C	C	C
XC2S600E	-6	-	-	-	C, I, Q	C, I
	-7	-	-	-	C	C

4. How does Xilinx compare in pricing in the Industrial temperature range?

For Industrial range devices, Xilinx FPGAs are typically 50% the cost of a comparable density device.

5. Will there be an extended temperature range for automotive applications?

Yes, all Spartan IIE devices, including the new extension parts will be offered as Automotive IQ devices and will be qualified at a junction temperature of -40°C to $+125^{\circ}\text{C}$. Q-grade devices will be offered in selected packages and slowest speed grade only.

6. What are the applications for IQ automotive products?

Xilinx IQ Solutions are designed for use in automotive applications such as GPS navigation systems, in-car entertainment, multimedia and driver assistance systems, digital audio broadcast (DAB) radios, adaptive cruise control, and other telematics and infotainment units. But can also be used in certain industrial and applications where extended temperature is needed for example test equipment in harsh environments, down hole applications and construction/agricultural equipment.

7. Will there be an increase in the available RAM in the new devices?

Yes. The XC2S400E has four columns of BRAM and the XC2S600E has six columns of BRAM that will increase the BRAM to 160K and 288K, respectively. Additionally, Xilinx will continue to be the only FPGA supplier to offer distributed RAM. The XC2S400E and XC2S600E will have an additional 150K and 216K of distributed RAM respectively.

8. What is the PROM support for two new devices?

Device	OTP PROM Solution	PD8	VO8	SO20	VQ44
XC2S50E	XC17S50A	✓	✓	✓	-
XC2S100E	XC17S100A	✓	✓	✓	-
XC2S150E	XC17S200A	✓	✓	-	✓
XC2S200E	XC17S200A	✓	✓	-	✓
XC2S300E	XC17S300A	-	-	-	✓
XC2S400E	XC17V04	-	-	-	✓
XC2S600E	XC17V04	-	-	-	✓

9. What software packages supports Spartan-IIE Devices?

The family extension will be supported in a special download based on ISE 5.1i Service Pack 3 and will be available at the time of Service Pack 3.

10. Will third party software be available?

Yes, we will provide the libraries and netlists for the new devices, and we will have them tested against our major partner's simulators (Modelsim, Cadence NC-Sim, and Synopsys VCS/Scirocco).

11. What kind of IP Support is available for Spartan-IIE?

Over 200 cores are available from the LogiCORE™ and AllianceCORE™ IP program. For a complete listing please go to <http://www.xilinx.com/search/ipsearch>

12. What is Field Programmable Controller (FPC)

The Xilinx FPC is a cost sensitive processing solution which includes the low cost Spartan-IIE FPGA family, coupled with the compact, high-performance MicroBlaze™ 32-bit RISC processor core. The solution includes the EDK with a wide assortment of peripherals and intellectual property, and full software support including compiler, assembler, and debugger, along with implementation, simulation and verification tools. The key advantages are:

- Customized Solution
 - You can easily create a customized processor-based design, and you can modify your design to meet changing requirements. You can also create one PC board that meets a wide range of different applications — just reconfigure the FPGA
- No Obsolescence
 - Xilinx allows you to purchase our MicroBlaze source code. This guarantees product availability for any application you choose. You can also port the core across Xilinx product lines or even target an ASIC

- **Lowest Cost Per I/O**
 - The Spartan FPGA devices contain up to 514 user I/O, with over 100% more capacity and the lowest cost per I/O than competing FPGAs in the same density ranges. This competitive advantage allows you to integrate more features while at the same time shrink the form factor for each device. Additionally, the greater I/O coverage gives you the advantages of high I/O count Gate Arrays with the added advantage of reprogrammability
- **Reduce Cost**
 - -By integrating your design onto a single device, you not only save time and effort, you also reduce your overall costs. Spartan-II FPGAs are the lowest cost programmable logic devices you can get, and they also give you another key advantage — reduced inventory costs; one device type can meet a broad range of uses in different products. Spartan-IIE FPGAs also allow you to integrate costly board-level features such as DLLs, RAM, and a variety of I/O translators into a single, compact, low cost platform.

13. What are the key points to remember about the Spartan-IIE family extension?

- Up to 600,000 gates and 514 I/Os
- Lowest cost FPGA in high volume production
- More available I/Os than competing devices
- Lowest cost per pin of any FPGA available today
- A cost sensitive solution for processing applications
- Four generations of low cost FPGAs with many more innovations to come

[For more FAQs about the Spartan-IIE Family, see FAQ100.](#)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/02/02	1.0	Initial Xilinx release.