Serial ATA I/II Host Controller (SATA_H1)

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ASICS World Services, LTD.

15559 Union Ave. Suite # 200
Los Gatos, CA 95032, U.S.A
Phone: 1 408 781-8043
Fax: 1 408 268-4173
E-mail: info@asics.ws
URL: www.asics.ws

AllianceCORE Facts

Provided with Core	
Documentation	User Manual
Design File Formats	EDIF netlist, Verilog
Constraints Files	sata_top.ucf
Verification	Test Bench, Test Vectors
Instantiation Templates	Verilog
Reference Designs & Application Notes	XAPP 716
Additional Items	
Simulation Tool Used	
ModelTech's Modelsim, Cadence NC-Verilog, CVER	
Support	
Support provided by ASICS World Services, LTD.	

Features

- 10 bit PHY interface
- Connects to SAPIS compliant serial ATA PHY
- Fully compliant to SATA Gen 1(1.5 Gbps) and Gen 2 (3.0 Gbps)
- WISHBONE, OPB or AHB slave interface for register access and FIFO/DMA data transfers
- 128 byte (32 double word) data FIFO (optional 256 byte)
- Implements the shadow register block and the serial ATA status and control registers
- Parallel ATA legacy software compatibility
- 48-bit address feature set supported
- 8b/10b coding and decoding
- CONT and data scramblers to reduce EMI
- CRC generation and checking
- Power management support (partial and slumber)
- Optional native mode programming model
- Many configuration options

Table 1: Example Implementation Statistics Xilinx® FPGAs

Family	Example Device	Fmax (MHz)	Slices[1]	IOB[2]	GCLK	BRAM	MULT/ DSP48	DCM / CMT	MGT	Design Tools
Virtex®-4	XC4VFX20-10	>110	2181	4	4	1	0	0	0	ISE® 10.1.01i
Virtex®-5	XCVLX50T-2	>110	996	4	4	1	0	0	0	ISE® 10.1.01i

Notes:

1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details

2) Assuming all core I/Os and clocks are routed off-chip

3) PHY Interface always runs on the 150 MHZ PHY Clock, independent of system bus speed

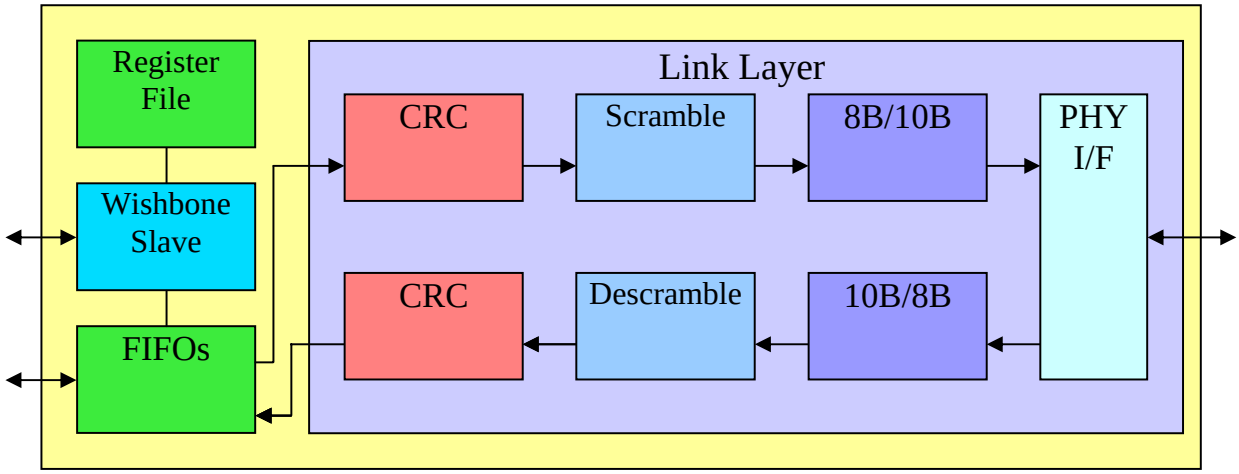

Figure 1: SATA_H1 Block Diagram

General Description

The AllianceCORE Serial ATA Host Controller provides an interface to high-speed serial link replacements for the parallel ATA attachment of mass storage devices. The serial link employed is a high-speed differential layer that utilizes Gigabit technology and 8b/10b encoding.

Functional Description

The Serial ATA Link and Transport Layer Core implements a serial ATA host interface which connects to a SATA PHY via a 10bit interface and provides a Wishbone slave interface for register and DMA access. It consists of the link layer module - with 10bit data paths to the physical layer - and a transport layer module which connects to the system via a Wishbone, OPB or AHB slave interface.

SAPIS PHY Interface

This interface connects to any SAPIS compliant serial ATA PHY. Power management and speed negotiation signals are included. The PHY interface is synchronous to the PHY clock domain, which may have a different clock frequency than the system clock domain. Synchronization is done by the Serial ATA Link and Transport Layer Core.

System Slave Interface

The slave interface is used to access all core internal registers as well as the data FIFO. Software or an external DMA unit can write transmit data into the data FIFO or can read from the FIFO. Interface wrappers for OHB and and AHB are available free of charge. PLB interface wrappers are currently in development.

DMA Handshake

Simple handshake signals are provided to connect a DMA unit to the core module. The DMA requests will be asserted as soon as any transmit data is available or is needed in the core's data FIFO. The DMA unit will then access the data FIFO via the Wishbone slave interface. A system interrupt will inform host software on completion of a data transfer.

Automatic flow control mechanisms control data throttling to avoid underflow or overflow of the transmit

data FIFO. The DMA unit (or host software) may work at any speed without the risk of data loss. Data FIFO thresholds can be adjusted to optimize the data flow control.

Core Modifications

System Interface can be one of:

- Wishbone
- OPB
- AHB

Recommended Design Experience

Basic understanding of Serial ATA and system design is required.

Ordering Information

This product is available directly from ASICS World Services, LTD. Please contact ASICS World Services, LTD. for pricing and additional information about this product. Contact information for them is on the front page of this data sheet.

Related Information

Additional Information and specifications such as Serial ATA specification may be obtained from:

Serial ATA Working Group
www.serialata.org

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com