SDRAM Controller, DDR (DDR-XS-XILINX)

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Array Electronics

Hachinger Weg 5
85649 Brunnthal
Germany
Phone: +49 8102-779784
Fax: +49 8102-779785
E-mail: info@array-electronics.com
URL: www.array-electronics.com

AllianceCORE™ Facts

Provided with Core	
Documentation	User Guide
Design File Formats	EDIF or NDC netlist, VHDL, Verilog
Constraints Files	UCF File
Verification	Test Bench
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	Reference Design included, adapted to core configuration
Additional Items	
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support Provided by Array Electronics	

Features

- Available under terms of the SignOnce IP License
- High performance memory access
- Full management of all 4 internal memory banks
  - Keeps row open after an access
  - All internal memory banks can be in the active state at any time
- Command queue architecture
- Optimised transaction processing with early activate and hidden precharge
- CAS latency, burst length and all memory timing parameters configurable
  - Supports CAS latencies of 2.0, 2.5 and 3.0
- Generic user application interface with split command and data busses
- Supports variable burst length in user command
- Support for DDR SDRAM devices from 64 Mbit to 1 Gbit

Table 1: Example Implementation Statistics

Family	Example Device	Fmax (MHz)	Slices[1]/ LUT- FF[2]	IOB[3]	GCLK	BUFIO	BRAM	DCM / CMT	MGT	PPC	Design Tools
Virtex™-5	XC5VLX30-1	250	1359	116	4	8	0	1	N/A	N/A	ISE 8.2.03i
Virtex-4	XC4VLX25-11	238	1115	116	4	8	0	1	N/A	N/A	ISE 8.2.03i
Spartan™-3	XC3S1000-5	147	1127	114	4	N/A	0	2	N/A	N/A	ISE 8.2.03i
Virtex-II Pro	XC2VP4-6	222	1048	114	4	N/A	0	2	N/A	N/A	ISE 8.2.03i

Notes:

1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details

2) Slices not reported for Virtex-5, so LUT-FF is used instead

3) Assuming only DDR SDRAM interface signals are routed off-chip with 64 bit data bus.

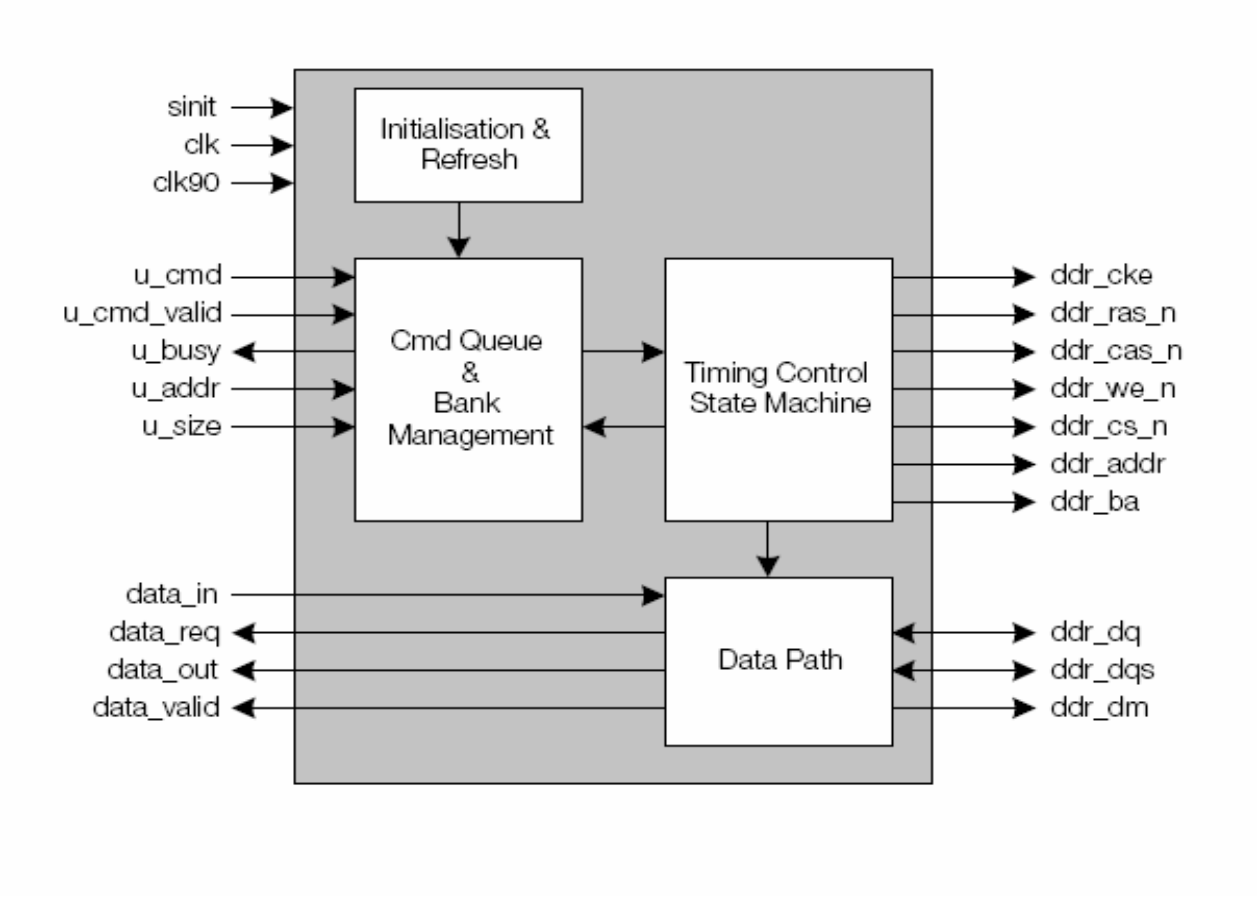

Figure 1: DDR SDRAM Controller XS Block Diagram

Features (continued)

- Uses ChipSync™ technology in Virtex-4 and Virtex-5 devices
  - Provides reliable read data capture with best timing margins
  - Supports the complete range of interface speeds from DDR166 to DDR400 used by DDR SDRAM devides
- Uses approved and reliable read data capture scheme in Spartan-3 and Virtex-II Pro devices
  - Generates source-synchronous read capture clock with the help of an external feedback loop and a second DCM
  - Supports interface speeds from DDR166 to DDR266 in Spartan-3 and DDR166 to DDR333 in Virtex-II Pro devices
- Fully synchronous design without asynchronous resets needs only a minimal set of timing constraints to achieve specified performance

Applications

- Digital image processing
- Streaming video and audio processing in consumer products and professional equipment
- Industrial data acqusition and control
- Measurement and test equipment in telecom and wired or wireless networking
- Medical and industrial ultrasonic inspection and analysis

General Description

The DDR SDRAM memory controller is a configurable high performance memory controller for systems requiring access to external DDR SDRAM memory devices or DDR DIMM modules with lowest latency and highest throughput. The controller consists of a high performance timing and control state machine that observes all timing requirements and issues the commands to the memory devices. The bank management module keeps track of the status of all the four internal banks of a DDR SDRAM device to minimize activate and precharge times. The command queue stores read or write requests until execution to optimize overall data throughput. There is no need to issue precharge, activate or refresh commands to the controller. All this functionality is handled internally by the controller.

Functional Description

Figure 1 depicts a block diagram of the DDR SDRAM Controller. The blocks are described in the following sections.

Command Queue and Bank Management Module

The user interface of the memory controller is split into a command bus and a separate data bus. This split allows for maximum flexibility while ensuring the highest performance during data transactions. The user command bus is connected to the command queue and bank management module of the controller. Read and write commands that are sent over the command bus are registered in a small command queue until the commands can be executed. The controller asserts a „busy“ signal if the command queue is full and cannot accept further commands. The busy signal will be deasserted once a command has been completed and there is space in the queue to accept another command. The amount of wait cycles that are introduced by the „busy“ signal are held as short as possible to prevent stall of command flow due to an empty or full command queue. The bank management logic keeps track of the currently open row in each of the internal memory banks and advices the controller whether a read or write command hits into a currently open row or whether the controller must open the row with a precharge command prior to execution of the read or write command.

Initialisation and Refresh Module

After power-up of the system, DDR SDRAMs require an initialisation sequence to reset internal logic and set certain operation parameters such as the burst length. After initialisation, the memory devices enter normal operation mode and can execute read and write requests to the internal memory array. During normal operation, refresh cycles must be applied periodically to ensure data integrity. The initialisation and refresh module of the controller performs the initialisation sequence according the recommendations from memory device vendors, ensuring successful power-up of the DDR SDRAMs without any additional user intervention. This module also contains the refresh counter, which periodically raises a refresh request in the controller. On a refresh request, the controller stops executing user commands, closes any open banks and issues a auto-refresh command to the memories. The controller then resumes execution of user commands.

Timing Control State Machine

The timing control state machine actually executes the read and write requests to the external memories while observing that the many DDR SDRAM timing requirements are completely satisfied. The module also issues the row activate and precharge commands to open or close a row within the addressed memory bank. The multi-banked architecture of DDR SDRAMs allow for several timing optimisations that the timing control state machine employs to completely or partially hide precharge or activate times, greatly improving the performance of the controller in many applications.

Datapath Module

Write data associated with a write command is sent in contiguous cycles to the controller over a separate write data bus. The controller will start the write process once the associated write command is at the head of the queue. There is a „write data request“ signal output from the controller indicating at which time the controller requires the write data. The write data is then forwarded to the memory data bus with minimum latency.

The controller sends read data associated with a read command in contiguous cycles to the user logic over a separate read data bus. A „read data valid“ signal from the controller indicates when the read data is available on the data bus. The data valid signal will be asserted for a number of contiguous clock cycles, consistent with the requested burst length.

Considering the tight timings of a DDR SDRAM memory interface, the capture of read data is a critical design aspect of a DDR SDRAM interface. The memory controller comes with two implementations of the read capture logic that are optimized for the target FPGA family and ensure the best timing margins and reliable data capture while keeping the need to constrain the design to a minimum. In Virtex-5 and Virtex-4 devices, the Xilinx ChipSync technology is used allowing the capture clock edges be placed precisely in the middle of the data valid window. In Spartan-3 and Virtex-II Pro FPGAs, the capture clock is generated by use of a second DCM that shifts the incoming clock from the external clock feedback loop by 90 degrees.

Address Mapping

The address bus from the user logic contiguously maps into the column, bank, row and chip select addresses of the memory devices with the column address being the least significant bits of the user address. This mapping achieves full bandwidth utilization for accesses with linear addressing scheme and for random accesses within a memory area that spans four contiguous rows.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
Clock and Reset Signals		
CLK	Input	Clock Input
CLK90	Input	Clock shifted by 90 degrees
DDR_RDATA_Clk	Input	Read data capture clock. This signal is the DDR SDRAM clock from the external feed back loop and delayed by 90° using a second DCM. The signal is only required when implementing the core in Virtex-II, Virtex-II Pro and Spartan-3 devices.
SINIT	Input	Reset signal. This input signal resets the whole memory controller and is synchronous with respect to clk.
INIT_DONE	Output	Initialisation sequence finished. The controller asserts this signal when it has finished the initialisation sequence of the DDR SDRAMs and enters normal operation. The signal is deasserted at reset of the controller and stays deasserted during the whole initialisation sequence.
User Interface Signals		
u_cmd(1..0)	Input	User Command. The command values are defined as following: 00 reserved

		01 READ – Execute a read access to memory 10 WRITE – Execute a write access to memory 11 reserved
u_cmd_valid	Input	User command valid signal. When asserted it indicates that u_cmd, u_addr and u_size are valid and can be accepted by the controller.
u_busy	Output	Busy signal. When this signal is asserted by the controller it indicates to the user logic that commands can not be accepted. If u_busy is not asserted and u_cmd_valid is asserted at the same clock edge the controller accepts a command for execution.
u_addr()	Input	User address. The address is the starting address of the read or write burst. See User Address Mapping for details of the mapping into the memory chip selects, bank, row and column addresses.
u_size(1:0)	Input	Burst length. This signal indicates the length of the read or write request. The burst length can be 1 to 4 words on the user data bus which corresponds to 2, 4, 6 or 8 data elements transferred over the DDR SDRAM data bus.
data_req	Output	Data request signal. When the controller executes a write command it asserts this signals for a contiguous number of clocks to request the data that will be written to memory.
data_in()	Input	Data input for write accesses. Data must be valid one clock cycle after data_req is asserted
data_vld	Output	Data valid signal. When the controller executes a read command it asserts this signal for a contiguous number of clocks when valid read data is available at data_out
data_out()	Output	Data output for read accesses. Read data is valid when data_valid is asserted.
DDR SDRAM Signals		
ddr_clk, ddr_clk_n	Output	Differential clock signal. The number of differential clock outputs can be configured with parameter C_NUM_DDR_CLK.
ddr_cs_n()	Output	Chip select signals. The number of chip select signals can be configured with the parameter C_DDR_CS_WIDTH.
ddr_cke()	Output	Clock enable. The number of clock enable signals is equal to the configured number of chip select signals. These signals should be actively pulled low at power-up and before the FPGA is configured to ensure correct power-up of the external memory devices.
ddr_ras_n, ddr_cas_n, ddr_we_n	Output	DDR SDRAM control signals
ddr_a()	Output	Address
ddr_ba(1..0)	Output	Bank address
ddr_dq()	Inout	Data bus
ddr_dqs()	Inout	Data strobe signals. In Virtex-II Pro and Spartan-3 devices, the data strobe signals are only used as output signals. In Virtex-5 and Virtex-4 devices, the data strobes are placed at BUFIO capable pins and used to capture read data.
ddr_reset_n	Output	Registered DIMM reset signal. This signal is available only if support for Registered DIMMs is enabled. See parameter C_REG_DIMM. This signal should be pulled down with an external resistor to ensure stable low level if FPGA is not yet configured.

Verification Methods

Functional correctness of the memory controller is validated using an extensive testbench and using memory models from major memory vendors. Read and write timing budget analysis has been done for Virtex-4, Virtex-II Pro and Spartan-3 FPGAs and using different memory configurations. Board-level timings have been extracted from analog simulation and verified with real hardware measurements using the Xilinx ML461 Memory Development Board and several in-house developed boards. The memory controller is in use by customers using Virtex-4, Spartan-3, Virtex-II Pro and Virtex-II devices and memory configurations from single point-to-point to multi-DIMM systems.

Recommended Design Experience

The user should be familiar with Xilinx design flows.

Available Support Products

A multi-ported user interface is available as an option to the base product allowing the user to easily manage several independent data streams in the design.

Ordering Information

This product is available directly from Xilinx Alliance Program member Array Electronics under the terms of the SignOnce IP License. Please contact Array Electronics for pricing and additional information about this product using the contact information on the front page of this datasheet. To learn more about the SignOnce IP License program, contact Array Electronics or visit the web:

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Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com