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AllianceCORE™ Facts

Provided with Core	
Documentation	Core Specifications, Instruction set details, test set details
Design File Formats	EDIF or NGC netlist , VHDL Source RTL available at extra cost
Constraints Files	chip_sdlc.ucf
Verification	Test bench, test vectors
Instantiation templates	VHDL, Verilog
Reference designs & application notes	Example Design Assembler programs
Additional Items	Simulation and synthesis scripts
Simulation Tool Used	
1076-Compliant VHDL Simulator	
Support	
Support provided by CAST, Inc.	

Features

- Based on Intel's 80C152 Global Serial Channel
- Flexible addressing schemes
  - Single and double byte address recognition
  - Address filtering allowing multicast and broadcast addresses
- 16-bit CCITT or 32-bit frame check sequence
- NRZ or NRZI data encoding
- Full or half duplex operation
- Automatic bit stuffing/stripping
- 3-byte internal receive and transmit FIFOs
- External or internally generated transmit and receive clocks
- Optional preamble generation
- Programmable interframe space
- Raw transmit and receive testing modes

Table 1: Example Implementation Statistics

Family	Example Device	Fmax[1] (MHz)	Slices	IOB[2]	GCLK	BRAM	MULT	DCM/ DLL	MGT	PPC	Design Tools
Virtex-II Pro™	XC2VP2-7	250	376	39	1	2	0	0	0	0	ISE 5.2.03i
Virtex-E™	XCV50E-8	139	383	39	1	2	N/A	0	N/A	N/A	ISE 5.2.03i
Virtex-II™	XC2V80-6	199	377	39	1	2	0	0	N/A	N/A	ISE 5.2.03i
Spartan-IIE™	XC2S50E-7	129	368	39	1	2	N/A	0	N/A	N/A	ISE 5.2.03i
Spartan-3™	XC3S200-4	109	376	39	1	2	0	0	N/A	N/A	ISE 5.2.03i

Notes:

1) Optimized for speed
2) Assuming all core I/O is routed off-chip

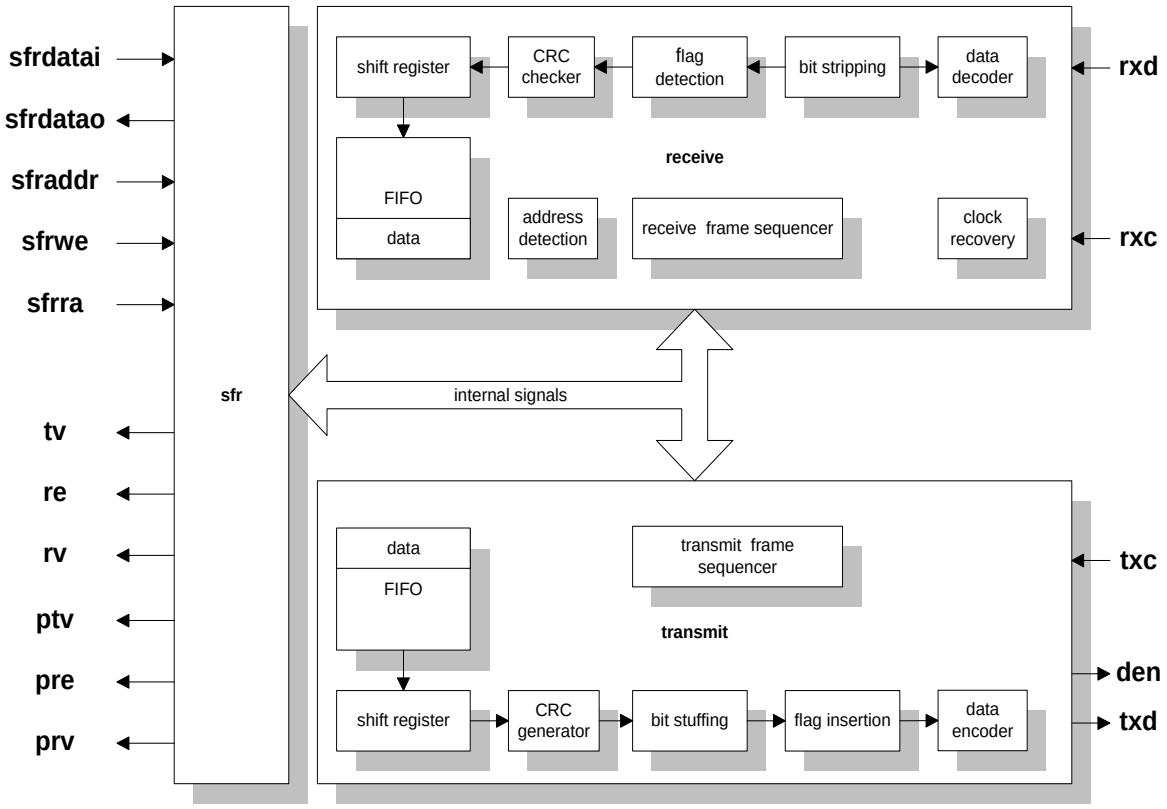

Figure 1: SDLC Controller Block Diagram

Applications

- ISDN D-channel
- X.25 networks
- Frame Relay networks
- Custom serial interfaces

General Description

The SDLC controller is a synthesizable HDL core of a high-speed synchronous serial communication interface.

Operation of the controller is similar to that used in Intel 8XC152 Global Serial Channel (GSC) working in SDLC mode under CPU control. Communication with CPU is realized through Special Function Registers (SFRs) and 3 interrupt sources. This allows the SDLC controller for an easy integration into any CPU core.

The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset; therefore scan insertion is straightforward.

Functional Description

The SDLC core is partitioned into modules as shown in figure 1 and described below.

SFR unit

This part is responsible for communication with the external host controller. In a typical application the external host may be a simple 8-bit embedded controller such as the 8051. Communication with that host is performed via a set of directly accessible 8-bit registers and 3 interrupt lines. These interrupts inform the external CPU about the ability for writing transmit data into the FIFO, reading just received data or about receive errors.

The SFR unit also contains a baud rate generator used by the Transmit and Receive units.

Transmit unit

This unit controls the transmit operation of the SDLC and is subdivided into several components responsible for generating properly formatted SDLC/HDLC frames. The whole unit is synchronous to the same global clock, which also feeds the SFR and Receive units.

The transmit frame sequencer is the main state machine responsible for generating all control signals used during frame formatting. Incoming data from the CPU goes directly into the transmit FIFO. After a transmit initialization sequence, the transmit frame sequencer automatically appends the HDLC frame flag and the optionally generated preamble sequence. It then periodically instructs the FIFO for writing data into the shift register.

After passing the shift register, the data goes to the crc generator, which computes the frame check sequence. Then the data goes to the bit stuffing unit which performs ones insertion procedure defined by the HDLC/SDLC protocol. The data encoder block forms data with NRZ or NRZI algorithms according to the current operating mode. If there is no transmit request, the Transmit unit can be idle or can generate a continuous idle flag sequence.

Receive unit

This unit controls the receive operation of the SDLC and is subdivided into several components responsible for receiving properly formatted SDLC/HDLC frames. The whole unit is synchronous to the same global clock, which also feeds the SFR and Transmit units.

Incoming data together with clock information passes through the data decoder which separates data from the incoming bit stream. The same bit stream also feeds the clock recovery unit, which detects and recovers the receiver clock signal. Decoded data goes through the bit stripping circuit to remove any appended zeros and then to the flag detector.

The flag detector recognizes flags defined by the HDLC/SDLC and indicates events such as the start of a new frame, end of a frame, abort or idle state on the line. This indication is used by the frame sequencer unit, the main state machine of the Receive component. After passing the flag detector, data goes to the crc checker unit and to the shift register. The frame sequencer periodically instructs the shift register to write data into the receive FIFO.

Core Modifications

The SDLC core can be modified to include features such as:

- Custom interfaces for external CPU
- Custom baud rate generation variants
- Variable size of internal FIFOs

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
Control Signal		
clk	in	Global clock
reset	in	Global reset
Special Function Registers interface		
sfrdatai	in	SFR data bus input
sfrdatao	out	SFR data bus output
sfraddr	in	SFR address bus
sfrwe	in	SFR write enable
sfrra	in	SFR read acknowledge
Interrupt sources		
rv	out	Receive valid interrupt
re	out	Receive error interrupt
tv	out	Transmit valid interrupt
Interrupt priorities		
prv	out	Receive valid priority
pre	out	Receive error priority
ptv	out	Transmit valid priority
Serial communication interface		
rxd	in	Receive input
txd	out	Transmit output
rxc	in	Receive clock
txc	in	Transmit clock
den	out	External driver enable

Verification Methods

The SDLC core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C152 chip, and the results compared with the core's simulation outputs.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

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