MW_ATSC

ATSC Modulator Core

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AllianceCORE Facts

Provided with Core	
Documentation	User Guide
Design File Formats	VHDL synthesizable source code, NGC implementation file
Constraints Files	Xilinx ISE User Constrains File
Verification	VHDL Test Bench and Test Vectors
Instantiation Templates	VHDL Wrapper
Reference Designs & Application Notes	MATLAB® Core Model and Spectrum Analyser
Additional Items	None
Simulation Tool Used	
ModelSim XE III, Aldec's Active-HDL	
Support	
Support and customization are provided by MindWay S.r.l	

Features

- Available under terms of the SignOnce IP License
- Fully compliant with ATSC A/53, including 16VSB modulation
- Support SMPTE 310 interface
- Support DVB-ASI interface
- Symbol rate locked to transport rate
- Sample rate independent on Symbol rate
- Status and control registers available for start up and continuous test and management
- Optional functionality:
  - ASI/SPI channel interface
  - Linear and Non-Linear Precorrection
  - Internal or external microcontroller interface

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family	Example Device	Fmax (MHz)	Slices	IOB[1]	GCLK	BRAM	MULT/ DSP48/E	DCM / CMT	MGT	Design Tools
Virtex®-4	XC4VSX35-10	139	10797	151	4	6	20	2	N/A	ISE® 9.2.04i
Virtex®-5	XC5VSX35-1	203	4879	151	4	6	18	2	N/A	ISE® 9.2.04i

Notes:

1) Assuming all core I/Os and clocks are routed off-chip

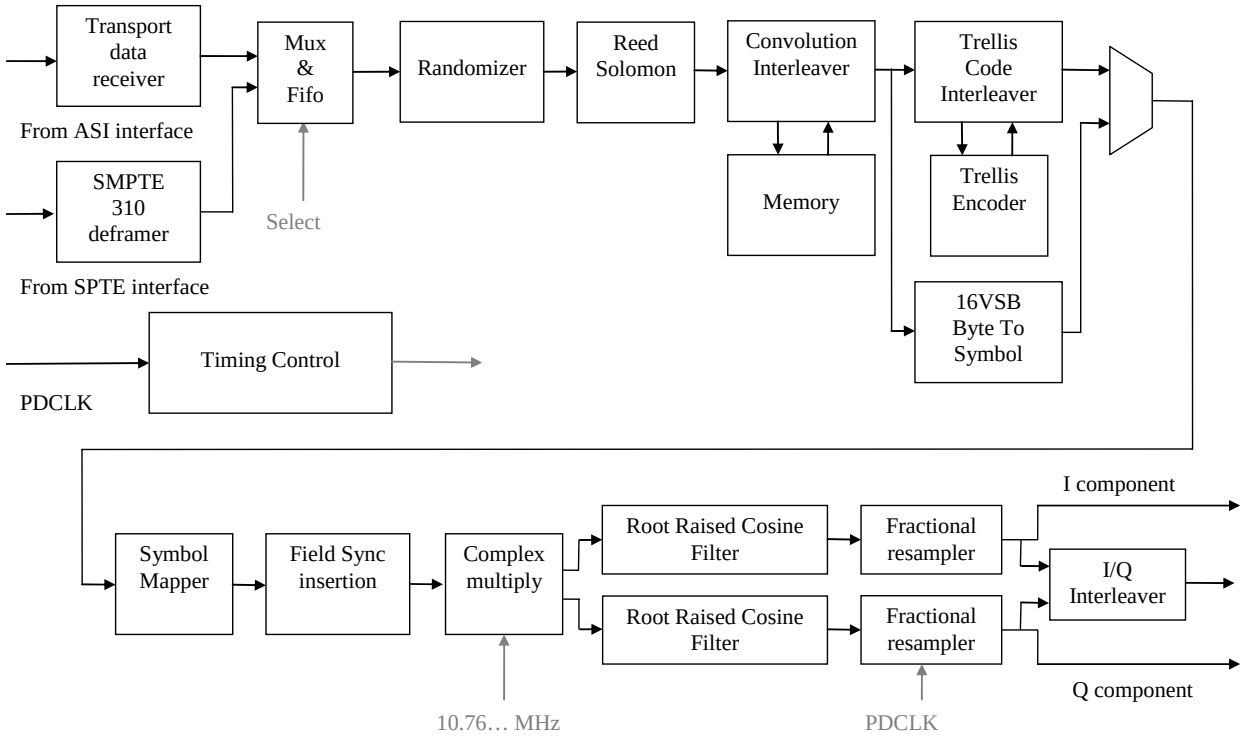

Figure 1: MW_ATSC Modulator Core Block Diagram

Applications

ATSC Transmission Systems

General Description

The MW_ATSC Modulator Core performs the digital baseband functions required for the transmission side of a 8-VSB Broadcasting link. The core implements the framing functions as defined by ATSC A/53, including the additional features for 16-VSB. It accepts a single, SMPTE 310 or DVB-ASI, MPEG-2 formatted transport stream and produces complex I/Q symbol pairs which should be supplied to an external upconverter.

Functional Description

Randomizer

This block receives an MPEG-2 transport packet and produces a randomized data stream, as defined at clause 6.4.1.1 of ATSC A/53.This block XOR's the incoming data bytes with a 16-bit pseudo random binary sequence (PRBS) generator which is initialized at beginning of a Data Field. The PRBS polynomial generator is: G(16) = X16 + X13 + X12 + X11 + X7 + X6 + X3 + X + 1. The sync byte of the incoming packet marks the beginning of Data Field, and the PRBS generator is loaded with the initialization value 0xF180.

Reed-Solomon Encoder

This block (clause 6.4.1.2 of ATSC A/53) is a Reed-Solomon encoder, RS(207, 187), that receives a 187 byte randomized transport packet and generates an error protected packet, adding 20 checksum bytes at the end of each packet to produce a total of 207 byte error protected data.

Main Service Interleaving

The data bytes (including the RS parity bytes) are interleaved. A convolutional byte-wide interleaver with depth 52 process the 207 byte coming from the Reed-Solomon encoder. Basically, it is composed by 52 delay lines, each one 4 bytes deeper then the previous. Branch 0 shows no delay. The first byte (Data Sync) of each 208 byte packet is passed through the branch 0, the next byte is stored into branch 1, the next into branch 2, etc. The sequence continues, and can be noted that 208 is divisible by 52, then it is guaranteed that sync byte always pass trough branch 0.

Trellis Coding

The 8-VSB transmission employs a 2/3 trellis code (with one unencoded bit which is precoded). That is, one input bit is encoded into two output bits using a one-half rate convolutional code while the other input bit is precoded. The signaling waveform used with the Trellis code is an 8-level (3 bit) one-dimensional constellation.

Trellis Code Interleaver

Clause 6.4.1.4 of ATSC A/53 specifies the Trellis code intrasegment interleaving. This uses twelve identical trellis encoders and precoders, operating on interleaved data symbols. The code interleaving is accomplished by encoding symbols (0, 12, 24, 36 ...) as one group, symbols (1, 13, 25, 37, ...) as a second group, symbols (2, 14, 26, 38, ...) as a third group, and so on for a total of 12 groups.

Data Sync

The MPEG-2 sync byte, which is referred as Data Sync is then replaced by 4-symbol Data Segment Sync, creating a complete data segment, consisting of 832 symbols: 4 symbols for Data Segment Sync, and 828 data plus parity symbols.

Field Sync insertion

Clause 6.5.2 of ATSC A/53 specifies also that data are not only divided into Data segments, but also in Data Fields, each consisting in 313 segments. That means that the ATSC Modulator inserts a full data field sync segment, 832 symbols long, containing one PN511 and tree PN63 patterns. The remaining symbols contain the VSB mode information plus 92 reserved symbol pattern.

Pilot Addition and vestigial sideband shaping

A small in-phase pilot is finally added to the data signal, adding a small dc level to every symbol.
A complex multiplier and two RRC filters provide the vestigial side band signal generation and guarantee the correct VSB system channel response (linear phase raised cosine filter).
The RRC filters provide also to keep the out of band signal at least 47 dB below the total transmitted power. See Figure 2 for MW_ ATSC Modulator Core emission mask.

Core Modifications

Source code uses VHDL generics in order to customize MW_ATSC Modulator Core. MindWay S.r.l. will provide support in order to integrate MW_ATSC Modulator Core into the final application.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
Clock and clear signals		
N_CLR	Input	Clear, active low
PDCLK	Input	Main Clock Operating at twice the Sample Rate
N_FLUSH	Input	Flush command, active low. Clear all internal logic
CLK_X_8_OUT	Out	System Clock Operating at 8 time (or up) the Symbol Rate
CLK_OUT	Out	Internal (after DCM) version of PDCLK
ASI channel		
TPD_IN(7:0)	Input	Transport Packet Data
TPD_VALID	Input	Transport Packet Data available, active high
SYNC_BYTE	Input	Sync Byte Indicator
READY_OUT	Output	Ready to receive new data, active high
SMPTE 310 channel		
SMPTE_IN	Input	SMPTE Biphase serial data
Settings		
CHANNEL_SEL	Input	Input channel select : 0 = ASI, 1 = SMPTE
MOD_16_VSB	Input	8_16 VSB selector : asserted when in 16-VSB mode
SR_MAIN_RATIO(23:0)	Input	Symbol frequency versus Main frequency ratio
TS_MAIN_RATIO(23:0)	Input	Transport frequency versus Main frequency ratio
I_FIRST	Input	Output I data component first if asserted
Flags		
SMPTE_CK_VLD	Output	SMPTE frequency valid, active high
SMPTE_T_IN_SYNC	Output	SMPTE In sync with the MPEG-2 incoming stream, active high
SMPTE_SYNC_OUT	Output	SMPTE Sync byte pulse
MUX_FIFO_OVFL	Output	Mux fifo Overflow
MUX_FIFO_UNFL	Output	Mux fifo Underrflow
FREQ_ERR	Output	Internal DDS Overflow/Underflow
FREQ_OFFST(10:0)	Output	Fifo level offset respect the Nominal value
FS_UNDERRUN	Output	Field Sync Inserter Fifo error
FF_UNDERRUN	Output	Fractional Filter Fifo error
FF_OVERRUN	Output	Fractional Filter Fifo error
N_CLR_FLG	Input	Flags clear, active Low
OFFSET(15:0)	Input	DC Offset
Data Out		
ATSC_OUT_VLD	Output	Data Out valid, active high
ATSC_I_OUT(15:0)	Output	Output data, I Component
ATSC_Q_OUT(15:0)	Output	Output data, Q Component
ATSC_I_NQ	Output	I/Q qualifier
ATSC_IQ_OUT(15:0)	Output	I and Q data out (Interleaved data)
ATSC_IQ_VALID	Output	I/Q data valid out, active high

Critical Signal Descriptions

In a typical application the MW_ ATSC Modulator Core directly interface with the upconverter and the same clock signal serves to syncronize both the input of data to the upconverter and the MW_ ATSC logic. In order to ensure correct timing relationship (setup/hold time requirements) at the input of data to the upconverter an OFFSET timig constraint is detailed into the Xilinx User Constraint File.

Verification Methods

Complete functional and timing simulation has been performed on the core. VHDL Test Bench and Simulation Vectors used for verification are provided with the core.

Recommended Design Experience

Users should be familiar with VHDL entry, synthesis, simulation and Xilinx design flows.

Available Support Products

Other blocks implementing additional signal processing functions (predistortion and filtering), input functions (ASI/SPI channel interface, PCR restamping, null packets removal/insertion) are available from MindWay S.r.l. in order to deliver complete ATSC high performances single chip applications.

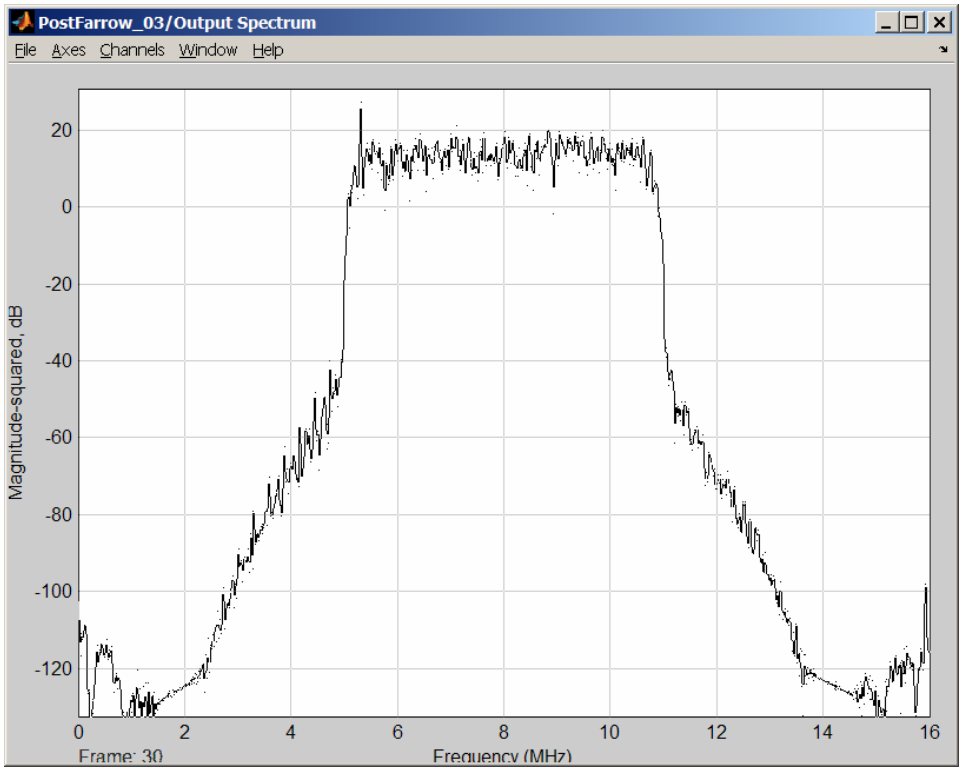

Figure 2: MW_ATSC Core Output Spectrum

Ordering Information

This product is available directly from Xilinx Alliance Program member MindWay S.r.l. under the terms of the SignOnce IP License. Please contact MindWay S.r.l. for pricing and additional information about this product using the contact information on the front page of this datasheet. To learn more about the SignOnce IP License program, contact MindWay S.r.l. or visit the web:

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Related Information

Xilinx Programmable Logic

ATSC A/53 ATSC Digital Television Standard Part 2 – RF/Transmission System Characteristics (A/53, Part 2:2007).

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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