MW_DVB-T/H

DVB Terrestrial/Handheld Modulator Core

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AllianceCORE Facts

Provided with Core	
Documentation	User Guide
Design File Formats	VHDL synthesizable source code, NGC implementation file
Constraints Files	Xilinx ISE User Constrains File
Verification	VHDL Test Bench and Test Vectors
Instantiation Templates	VHDL Wrapper
Reference Designs & Application Notes	MATLAB® Core Model and Spectrum Analyser
Additional Items	None
Simulation Tool Used	
ModelSim XE III, Aldec's Active-HDL	
Support	
Support and customization are provided by MindWay S.r.l	

Features

- Available under terms of the SignOnce IP License
- Fully compliant with ETSI EN 300 744 V1.5.1 (2004-11)
- Support DVB-H functionality (ETSI EN 300 744 V1.5.1 (2004-11) - annex F)
- Configurable for 2K, 4K and 8K Transmission Modes
- Support Hierarchical Transmission Mode
- Status and control registers available for start up and continuous test and management
- Internal 20 bit architecture for high level MER and BER performances
- Options:
  - SFN synchronization
  - ASI/SPI channel interface
  - Linear and Not Linear Precorrection
  - Out-of-band spectral mask filtering (clause 4.8.2 ETSI EN 300 744 V1.5.1 (2004-11))
  - Internal or external µ-controller interface

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family	Example Device	Fmax (MHz)	Slices	IOB[1]	GCLK	BRAM	MULT/ DSP48/E	DCM / CMT	MGT	Design Tools
Spartan™-3	XC3S4000-4	78	4585	135	1	68	12	0	N/A	ISE™ 9.2.04i
Virtex™-4	XC4VLX40-10	106	4494	135	1	68	12	0	N/A	ISE™ 9.2.04i
Virtex™-5	XC5VLX50-1	142	1935	135	1	34	12	0	N/A	ISE™ 9.2.04i

Notes:

1) Assuming all core I/Os and clocks are routed off-chip

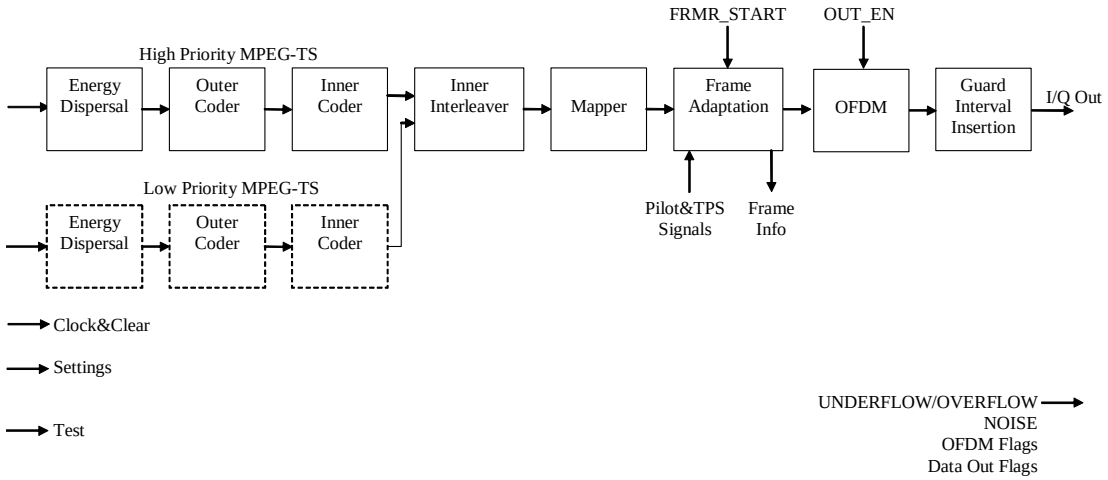


Figure 1: MW_DVB-T/H Modulator Core Block Diagram

Applications

DVB Terrestrial/Handheld Transmission Systems

General Description

The MW_DVB-T/H Modulator Core performs the digital baseband functions required for the transmission side of a Digital Video Broadcasting Terrestrial link. The core implements the framing functions as defined by ETSI EN 300 744 V1.5.1 (2004-11), including the additional features for DVB-H as defined in the annex F. It accepts a single, or pair in hierarchical transmission mode, MPEG-2 formatted transport stream(s) and produces complex I/Q symbol pairs which should be supplied to an external upconverter.

Functional Description

Energy Dispersal

This block receives an MPEG-2 transport packet and produces a randomized data stream, as defined at clause 4.3.1 of ETSI EN 300 744 V1.5.1 (2004-11).This block inverts a sync byte every eight sync byte received.The polynomial for the pseudo random binary sequence (PRBS) generator is: $1 + x^{14} + x^{15}$. The sync byte of the first packet is bit-wise inverted from 47_{HEX} to $B8_{HEX}$, and the PRBS generator is loaded with the seed sequence “100101010000000”. During the MPEG-2 sync bytes of the subsequent seven trasport packets the PRBS generator continues, but its output is disabled, leaving the sync bytes unchanged. Thus the period of the PRBS sequence is 1503 bytes.

Outer Coder

This block (clause 4.3.2 of ETSI EN 300 744 V1.5.1 (2004-11)) is a Reed-Solomon encoder, RS(204, 188), that receives a 188 byte randomized transport packet and generates an error protected packet,

adding 16 checksum bytes at the end of each packet to produce a total of 204 byte error protected data. Then a convolutional byte-wide interleaver with depth I=12 process the 204 byte coming from the Reed-Solomon encoder. Basically, it is composed by 12 delay lines, each one 17 bytes deeper then the previous. Branch 0 shows no delay. The first byte (sync) of each 204 byte packet is passed through the branch 0, the next byte is stored into branch 1, the next into branch 2, etc. The sequence continues, and can be noted that 204 is divisible by 12, then it is guaranteed that sync byte always pass trough branch 0.

Inner Coder

This block allows for a range of puntured convolutional codes, based on a mother convolutional code of rate 1/2 with 64 states. This allow selection of the most appropriate level of error correction. The generator polynomials of the mother code are $G_1=171_{OCT}$ for X output and $G_2=133_{OCT}$ for Y output. The two bit stream, X and Y, are punctured accordingly the desired code rate (1/2, 2/3, 3/4, 5/6 or 7/8).Table 2 of ETSI EN 300 744 V1.5.1 (2004-11) describes this functionality.

Inner Interleaver

Clause 4.3.4 of ETSI EN 300 744 V1.5.1 (2004-11) specifies a block based bit interleaver concatenated with a symbol interleaver. If Hierarchical Transmission Mode is selected then the two streams are merged at this point with a modified interleaving equation.

Mapper

This bock performs the constellations and mapping using the mapping schemes specified by clause 4.3.5 of ETSI EN 300 744 V1.5.1 (2004-11) for QPSK, 16-QAM or 64-QAM. It outputs I/Q symbol pairs stream to the IFFT.

Frame Adaptation

Clause 4.5 and 4.6 of ETSI EN 300 744 V1.5.1 (2004-11) specifies a frame and super-frame structure with scattered, continuous and TPS pilots inserted at various carriers within each symbol. This block manages the pilot insertion dependent on the selected Transmission Mode (2K, 4K or 8K). TPS values are read by the Frame Adaptation logic at the beginning of each symbol. The external logic is in charge to change the TPS value at the correct time, that is at the beginning of a frame. Internal logic generates a set of output strobes which can be used to monitor such timings.

OFDM

This block performs the Inverse Fast Fourier Transform (IFFT) on the carriers.

Guard Interval Insertion

This block manages the on-air timing of the OFDM symbols by guard interval insertion.

Core Modifications

Source code uses VHDL generics in order to customize MW_DVB-T/H Modulator Core. MindWay S.r.l. will provide support in order to integrate MW_DVB-T/H Modulator Core into the final application.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
Clock and Clear signals		
N_CLR	Input	Clear, active low
CLK_X_8	Input	Main Clock Operating at 8 time the Symbol Rate
N_FLUSH	Input	Flush command, active low. Clear all internal logic
High Priority channel		
TPD_IN_HP(7:0)	Input	High priority Transport Packet Data
TPD_VALID_HP	Input	High priority Transport Packet Data available, active high
SYNC_1_HP	Input	High priority Sync Byte 1 Indicator
SYNC_BYTE_ HP	Input	High priority Sync Byte Indicator
RATE_SEL_HP(2:0)	Input	High priority Code Rate Select
READY_OUT_HP	Output	High priority Ready to receive new data, active high
Low Priority channel (active only if working in Hierachical mode)		
TPD_IN_ LP (7:0)	Input	Low priority Transport Packet Data
TPD_VALID_ LP	Input	Low priority Transport Packet Data available, active high
SYNC_1_ LP	Input	Low priority Sync Byte 1 Indicator
SYNC_BYTE_ LP	Input	Low priority Sync Byte Indicator
RATE_SEL_LP(2:0)	Input	Low priority Code Rate Select
READY_OUT_LP	Output	Low priority Ready to receive new data, active high
Framer Control		
FRMR_START	Input	Framer start
Settings		
H_MODE_EN	Input	Hierarchical mode enable
C_ORDER(1:0)	Input	Code Rate Select
ALPHA(2:0)	Input	Constellation Uniformity (Alpha parameter)
S_MODE(1:0)	Input	Symbol Interleaver Mode
T_MODE(1:0)	Input	Transmission Mode (Active carriers per OFDM symbol)
GUARD(1:0)	Input	Guard Interval
TPS related info		
TPS_S_MODE(1:0)	Input	TPS Symbol Interleaver Mode
TPS_T_MODE(1:0)	Input	TPS Transmission Mode (Active carriers per OFDM symbol)
TPS_H_MODE_EN	Input	TPS Hierarchical mode enable
TPS_RATE_SEL_HP(2:0)	Input	TPS Code Rate Select
TPS_RATE_SEL_LP(2:0)	Input	TPS Code Rate Select
TPS_C_ORDER(1:0)	Input	TPS Constellation order
TPS_ALPHA(2:0)	Input	TPS Constellation Uniformity (Alpha parameter)
TPS_GUARD(1:0)	Input	TPS Guard Interval

TPS_CELL_ID_EN	Input	TPS Enable sending of Cell identifier
TPS_CELL_ID (15:0)	Input	TPS Cell identifier
TPS_DVB_H_EN	Input	TPS DVB-H Signalling enable
TPS_DVB_H_SRVC_HP(1:0)	Input	TPS DVB-H Service indication for HP channel
TPS_DVB_H_SRVC_LP(1:0)	Input	TPS DVB-H Service indication for LP channel
Framer related info		
TPS_EOS_FLAG	Output	Framer End of Symbol
FRMR_S_START	Output	Begin of Framer OFDM Symbol
FRMR_F_START	Output	Begin of Framer OFDM Frame
FRMR_SF_START	Output	Begin of Framer OFDM Super Frame
Flags		
IFFT_OVERFLOW	Output	IFFT Overflow
NOISE_HP	Output	High priority Outer Interleaver Data out contains noise
NOISE_LP	Output	Low priority Outer Interleaver Data out contains noise
OFDM_SYMBOL_OUT	Output	Begin of OFDM Symbol
OFDM_FRAME_OUT	Output	Begin of OFDM Frame
Test		
BLANK_SPNT(12:0)	Input	Carriers Hole start point
DVB-T/H control		
OUT_EN	Input	DVB-T Output enable, active high
Z_OUT(19 : 0)	Output	Real and Imaginary Data Output
RL_NIM	Output	Real / Imaginary Data Output qualifier
Z_OUT_VALID	Output	Data Output available, active high
Z_OUT_NZ	Output	Not Zero forced Data Output value
EMPTY_DATA	Output	No data valid on output

Critical Signal Descriptions

In a typical application the MW_DVB-T/H Modulator Core directly interface with the upconverter and the same clock signal serves to syncronize both the input of data to the upconverter and the MW_DVB-T/H logic. In order to ensure correct timing relationship (setup/hold time requirements) at the input of data to the upconverter an OFFSET timig constraint is detailed into the Xilinx User Constraint File.

Verification Methods

Complete functional and timing simulation has been performed on the core. VHDL Test Bench and Simulation Vectors used for verification are provided with the core.

Recommended Design Experience

Users should be familiar with VHDL entry, synthesis, simulation and Xilinx design flows.

Available Support Products

A complete ETSI EN 300 744 V1.5.1 (2004-11) compliant DVB-T/H high performances single chip applications is available from MindWay S.r.l., as input functions ASI/SPI channel interface, PCR restamping, null packets removal/insertion (MW_DVB-T/H_A), additional signal processing functions (Linear and Non-Linear Precorrection) (MW_DVB-T/H_FP) or Single Frequency Network synchronization (SFN) (MW_DVB-T/H_S).

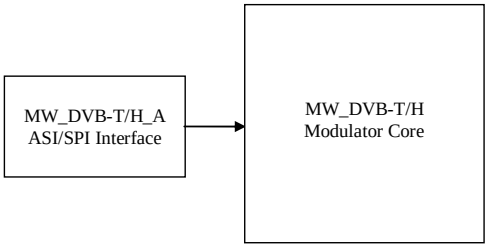


Figure 2: DVB-T Transmitter

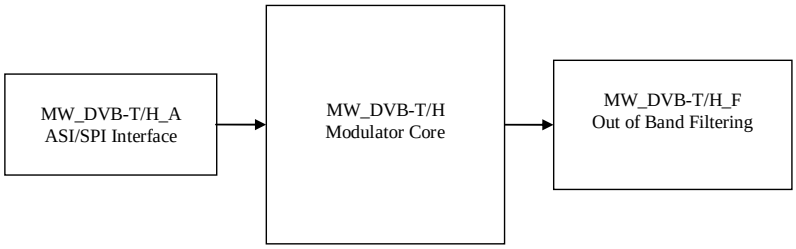
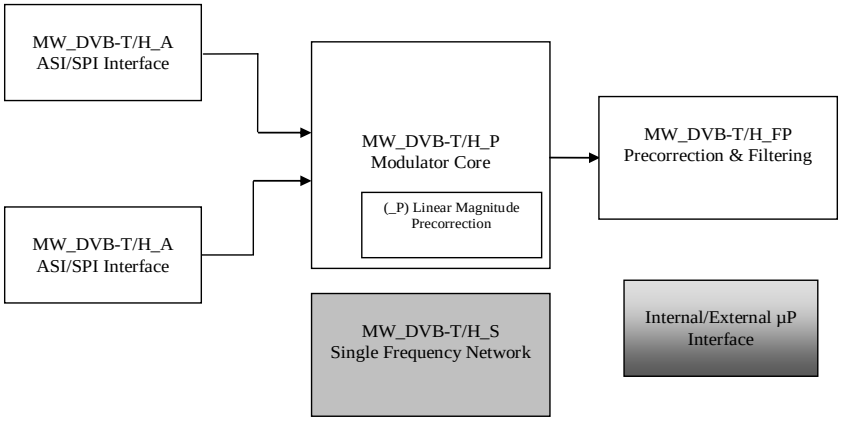


Figure 3: DVB-T Transmitter co-sited and operating on a channel adjacent to a transmitter for analogue television



Notes:

1) Linear Magnitude Precorrection functionality is implemented as part of the DVB-T/H Modulator Core (MW_DVB-T/H_P) because it processes OFDM symbol carriers before the IFFT block.

Figure 4: High-End DVB-T/H Transmitter

Ordering Information

This product is available directly from Xilinx Alliance Program member MindWay S.r.l. under the terms of the SignOnce IP License. Please contact MindWay S.r.l. for pricing and additional information about this product using the contact information on the front page of this datasheet. To learn more about the SignOnce IP License program, contact MindWay S.r.l. or visit the web:

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Related Information

Industry Information

ETSI EN 300 744 v1.5.1 (2004-11) Digital Video Broadcasting (DVB); Framing structure, channel coding and modulation for terrestrial television.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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