MW_DVB-T/H_A

ASI/SPI Interface Core

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AllianceCORE Facts

Provided with Core	
Documentation	User Guide
Design File Formats	VHDL synthesizable source code, NGC implementation file
Constraints Files	Xilinx ISE User Constrains File
Verification	VHDL Test Bench and Test Vectors
Instantiation Templates	VHDL Wrapper
Reference Designs & Application Notes	MATLAB® Core Model and Spectrum Analyser
Additional Items	None
Simulation Tool Used	
ModelSim XE III, Aldec's Active-HDL	
Support	
Support and customization are provided by MindWay S.r.l	

Features

- Available under terms of the SignOnce IP License
- Transport Stream rate adaptation by NULL Transport Stream Packets removal/insertion
- Support Transport Stream input data rate from 3.5Mbit/s to 35Mbit/s
- 188-byte and 204-byte Transport Stream Packets supported
- Input Transport Stream data rate monitoring
- PCR restamping
- Status and control flags available for start up and continuous test and management

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family	Example Device	Fmax (MHz)	Slices	IOB[1]	GCLK	BRAM	MULT/ DSP48/E	DCM / CMT	MGT	Design Tools
Spartan™-3x	XC3S4000-4	54	1034	51	3	4	0	0	N/A	ISE™ 9.2.04i
Virtex™-4	XC4VLX40-10	54	1043	51	3	4	0	0	N/A	ISE™ 9.2.04i
Virtex™-5	XC5VLX50-1	54	518	51	3	4	0	0	N/A	ISE™ 9.2.04i

Notes:

1) Assuming all core I/Os and clocks are routed off-chip

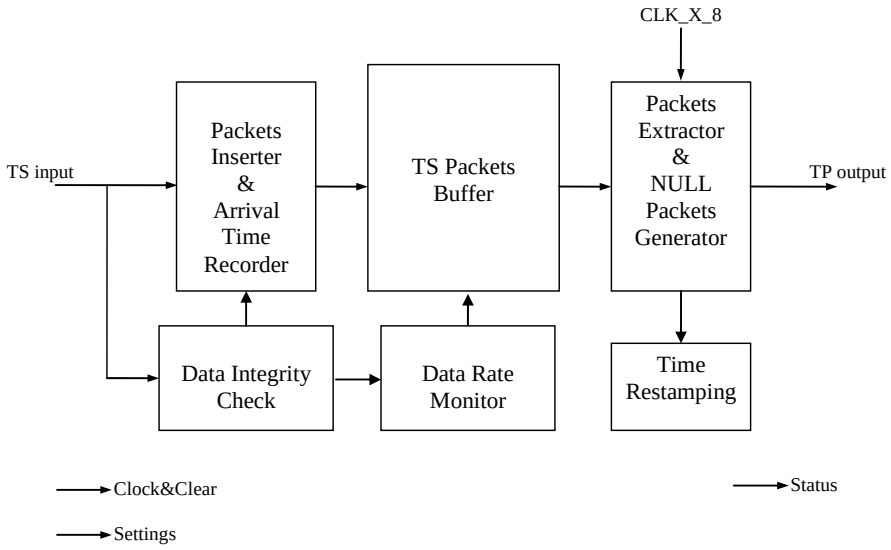


Figure 1: MW_DVB-T/H_A Block Diagram

Applications

DVB Transmission Systems

General Description

The MW_DVB-T/H_A Interface Core performs Transport Stream rate adaptation receiving MPEG-2 Transport Stream data from an ASI or SPI input channel receiver and providing a constant and continuous data stream to the MW_DVB-T/H Modulator Core, in order to match the required modulator on-air Symbol Rate. Thus it is possible for the input Transport Stream rate to be greater than the required on-air rate provided the true Transport Stream packet content (i.e. non NULL TS packets) is still less than the on-air rate.The interface removes incoming NULL packets and store the meaningful packets in a temporary buffer. When the MW_DVB-T/H Modulator Core is ready to receive new data, if in the buffer there is a complete Transport Packet, the packet is trasferred to the DVB-T/H modulator, otherwise a NULL packet is generated. The MW_DVB-T/H_A Interface Core allows Transport Stream data to be input at any rate from 3.5Mbit/s to 35Mbit/s.

Functional Description

Packets Inserter & Arrival Time Recorder

This block temporarily stores the incoming TS packets and detects NULL TS packets. The Arrival Time Recorder extracts PCR and records the arrival time of each TS.

Data Integrity Check

This block implements a synchronization process based on the TS packet length (188 or 204 byte). Any change of the packet length causes a resynchronization process with a temporary synchronization loss. If enabled, it detects automatically the input packet length.

Data Rate Monitor

This block implements a data rate dejitter function which computes the average TS packets rate using the average period of last 256 TS input packets, in order to define the correct ideal arrival time and to make available to the output TS packets at the highest possible regular rate. If this monitoring is disabled internal logic uses incoming TS packets rate.

TS Packets Buffer

This block extracts temporarily stored incoming TS packets, it removes NULL TS packets and it mades each meaningful TS packet available to the output logic.

Packets Extractor & NULL Packets Generator

This block outputs a continuous data stream. If there is a complete Transport Packet in the TS Packets Buffer the packet is transferred in output, otherwise a NULL packets is inserted.

Time Restamping

This block ensures that the TS PCR values are corrected for the additional NULL TS packets inserted. The internal time unit for PCR correction is clocked by a 27MHz reference clock.

Core Modifications

Source code uses VHDL generics in order to customize MW_DVB-T/H_A Interface Core. MindWay S.r.l. will provide support in order to integrate MW_DVB-T/H_A Interface Core into the final application.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
Clock and Clear signals		
N_CLR	Input	Clear, active low
CLK_X_8	Input	MW_DVB-T/H Modulator Core Main Clock
REFCLK	Input	ASI/SPI Input Channel Receiver Reference Clock [1)]
ASI/SPI Input Channel Receiver Interface		
Q_DATA[7:0]	Input	Parallel Data Input

SC	Input	Special Character (ASI mode only)
RVS	Input	Received Violation Symbol (ASI mode only)
Q_SYNC	Input	Sync Character (SPI mode only)
Q_RDY	Input	Parallel Data Input Ready
CKR	Input	Clock Read from ASI/SPI Input Channel receiver
Settings		
MODE_204	Input	Transport Stream Packet length Select
PKT_LEN_EN	Input	Transport Stream Packet length detection Enable
BIT_RTE_EN	Input	Transport Stream Packet rate monitor Enable
BIT_RTE_START	Input	Transport Stream Packet rate monitor Start
PCR_EN	Input	PCR restamping Enable
NULL_D_EN	Input	Transport Stream NULL Packet automatic discard Enable
Status		
IN_SYNC	Output	Transport Stream Packet length correct
DATA_RCVD	Output	Transport Stream Packet received
NULL_RCVD	Output	Transport Stream NULL Packet received
SYNC_ERR	Output	Transport Stream Packet length error
TP_LEN	Output	Transport Stream Packet length (0 – 188 bytes, 1 - 204 bytes)
TS_OVERRUN	Output	Transport Stream Packet Buffer Overrun
BIT_RATE_LOCKED	Output	Transport Stream Packet rate monitor locked
OVERRUN	Output	Transport Stream Packets Inserter Overrun
UDERRUN	Output	Transport Stream Packets Inserter Underrun
BIT_RATE_LOW	Output	Transport Stream Packet input rate too low for Data Rate Monitor computation logic
CLEAR_FLAG	Input	Clear Registered Status Flags, active high
R_SYNC_ERR	Output	Registered SYNC_ERR Status Flag
R_TS_OVERRUN	Output	Registered TS_OVERRUN Status Flag
R_OVERRUN	Output	Registered OVERRUN Status Flag
R_UNDERRUN	Output	Registered UNDERRUN Status Flag
R_BIT_RATE_LOW	Output	Registered BIT_RATE_LOW Status Flag
Transport Packet Output		
RDY_IN	Input	Ready to receive from MW_DVB-T/H Modulator Core
TPD[7:0]	Output	Transport Packet Data Output
TPD_VALID	Output	Transport Packet Data Output Available
SYNC_1	Output	Transport Packet Data Output Sync Byte 1 Indicator
SYNC_BYTE	Output	Transport Packet Data Output Sync Byte Indicator
NULL_PKT	Output	Transport Packet NULL Packet Inserted Indicator
TPKT_AVAIL	Output	Transport Packet (non NULL Packet) Available

Notes:

1) REFCLK is used also as System Clock by MW_DVB-T/H_A Interface Core and as Clock by time unit for PCR correction. It is supposed to run at 27MHz ± 30 ppm.

Verification Methods

Complete functional and timing simulation has been performed on the core. VHDL Test Bench and Simulation Vectors used for verification are provided with the core.

Recommended Design Experience

Users should be familiar with VHDL entry, synthesis, simulation and Xilinx design flows.

Available Support Products

A complete ETSI EN 300 744 V1.5.1 (2004-11) compliant DVB-T/H high performances single chip applications is available from MindWay S.r.l., as DVB-T/H Modulator Core (MW_DVB-T/H_P), additional signal processing functions (Linear and Non-Linear Precorrection) (MW_DVB-T/H_FP) or Single Frequency Network synchronization (SFN) (MW_DVB-T/H_S).

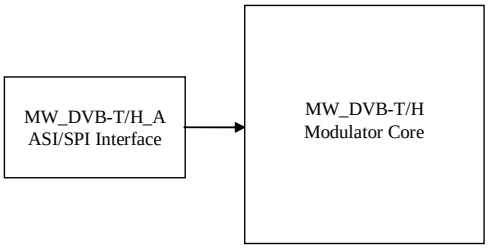


Figure 2: DVB-T Transmitter

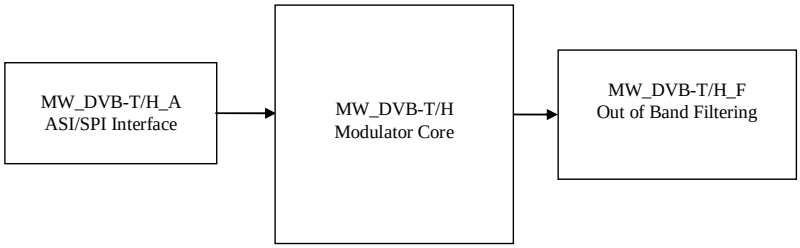
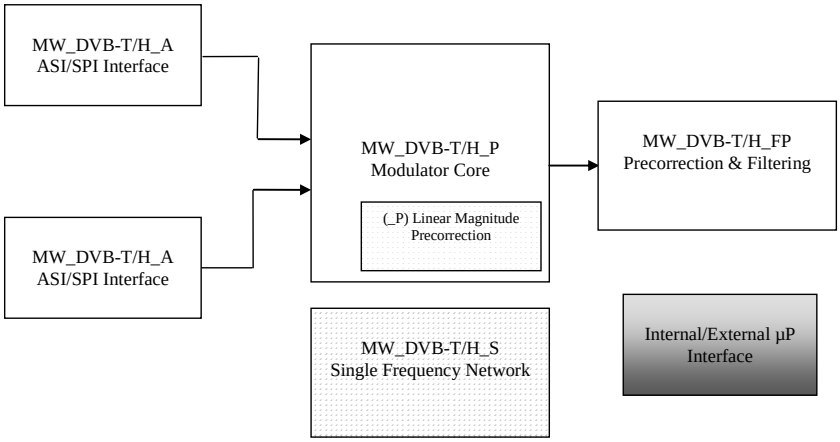


Figure 3: DVB-T Transmitter co-sited and operating on a channel adjacent to a transmitter for analogue television



Notes:

1) Linear Magnitude Precorrection functionality is implemented as part of the DVB-T/H Modulator Core (MW_DVB-T/H_P) because it processes OFDM symbol carriers before the IFFT block.

Figure 4: High-End DVB-T/H Transmitter

Ordering Information

This product is available directly from Xilinx Alliance Program member MindWay S.r.l. under the terms of the SignOnce IP License. Please contact MindWay S.r.l. for pricing and additional information about this product using the contact information on the front page of this datasheet. To learn more about the SignOnce IP License program, contact MindWay S.r.l. or visit the web:

Email: commonlicense@xilinx.com
URL: www.xilinx.com/ipcenter/signonce

Related Information

Industry Information

ETSI EN 300 744 v1.5.1 (2004-11) Digital Video Broadcasting (DVB); Framing structure, channel coding and modulation for terrestrial television.

EN 50083-9 Cabled distribution systems for television, sound and interactive multimedia signals. Part 9: Interfaces for CATV/SMATV headends and similar professional equipment for DVB/MPEG-2 transport streams.

ISO/IEC 13818-1 Information technology – Generic coding of moving pictures and associated audio information: Systems

ETSI TR 101 891 v1.1.1 (2001-01) Digital Video Broadcasting (DVB); Professional Interfaces: Guidelines for the implementation and usage of the DVB Asynchronous Serial Interface (ASI).

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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