MW_DVB-T/H_F

DVB Terrestrial/Handheld Filter Core

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AllianceCORE Facts

Provided with Core	
Documentation	User Guide
Design File Formats	VHDL synthesizable source code, NGC implementation file
Constraints Files	Xilinx ISE User Constrains File
Verification	VHDL Test Bench and Test Vectors
Instantiation Templates	VHDL Wrapper
Reference Designs & Application Notes	MATLAB® Core Model and Spectrum Analyser
Additional Items	None
Simulation Tool Used	
ModelSim XE III, Aldec's Active-HDL	
Support	
Support and customization are provided by MindWay S.r.l	

Features

- Available under terms of the SignOnce IP License
- Compliant with European Telecommunications Standard ETSI EN 300 744 V1.5.1 (2004-11)
- Filtering of out-of-band spectral spreeding compliant to clause 4.8.2 of ETSI EN 300 744 V1.5.1 (2004-11)
- Optional internal or external microcontroller interface could be added

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family	Example Device	Fmax (MHz)	Slices	IOB[1]	GCLK	BRAM	MULT/ DSP48/E	DCM / CMT	MGT	Design Tools
Spartan™-3x	XC3S4000-4	77	5950	87	2	0	6	0	N/A	ISE™ 9.2.04i
Virtex™-4	XC4VLX100-10	81	5950	87	2	0	6	0	N/A	ISE™ 9.2.04i
Virtex™-5	XC5VLX220-1	81	2955	87	2	0	6	0	N/A	ISE™ 9.2.04i

Notes:

1) Assuming all core I/Os and clocks are routed off-chip

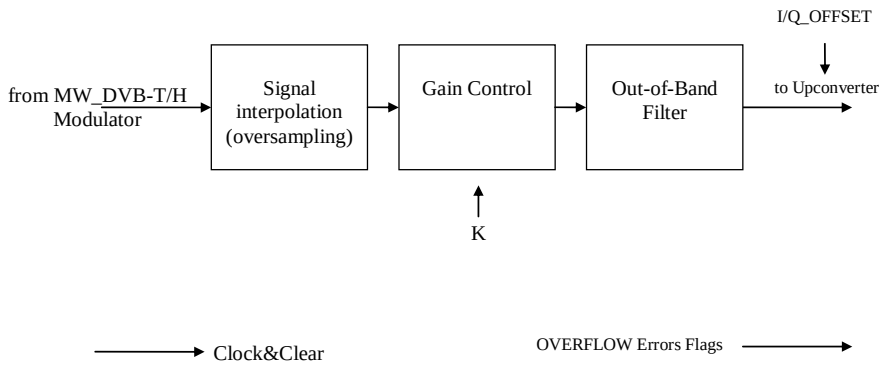


Figure 1: MW_DVB-T/H_F Filter Core Block Diagram

Applications

DVB Terrestrial/Handheld Transmission Systems

General Description

The MW_DVB-T/H_F Filter Core performs Gain Control and Out-of-Band Filtering, receiving data from MW_DVB-T/H Modulator Core and providing complex I/Q symbol pairs which should be supplied to an external upconverter.

Functional Description

Signal Interpolation

Signal Interpolation block is implemented as a fixed 4X interpolator filter. Signal gain control and low-pass filter for out-of-band removal should operate at higher rate than symbol rate in order to limit in band degradation caused by aliasing.

Gain Control

This block scales signal amplitude in order to make optimum use of full available dynamic range.

Out-of-Band Filter

This block limits the out-of-band spectral spreading (Spectrum Shoulders) outside the nominal bandwidth for cases where the DVB-T/H transmitter is co-sited and operating on a channel adjacent to a transmitter

for analogue television, in order to meet spectral mask requirement specified by clause 4.8.2 of ETSI EN 300 744 V1.5.1 (2004-11)

Core Modifications

Source code uses VHDL generics in order to customize MW_DVB-T/H_F Filter Core. MindWay S.r.l. will provide support in order to integrate MW_DVB-T/H_F Filter Core into the final application.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
Clock and clear signals		
N_CLR	Input	Main Clear, active low
CLK_X_8	Input	Main Clock Operating at 8 time the Symbol Rate
CLK_X_16	Input	Secondary Clock
Control signals		
Q_OFFSET(7:0)	Input	User defined Real Data Offset
I_OFFSET(7:0)	Input	User defined Imaginary Data Offset
Gain Control signals		
K (19:0)	Input	User Gain Factor
Overflow Error Flags		
INT_R_OVFL	Output	Interpolator's Overflow error flag on Real Data
INT_I_OVFL	Output	Interpolator's Overflow error flag on Imaginary Data
RCT_R_OVFL	Output	Clipper's Overflow error flag on Real Real Data
RCT_I_OVFL	Output	Clipper's Overflow error flag on Imaginary Data
SHLR_R_OVFL	Output	Out-of-Band filter's Overflow error flag on Real Data
SHLR _I_OVFL	Output	Out-of-Band filter's Overflow error flag on Imaginary Data
MW_DVB-T/H Modulator Core Interface signals		
EMPTY_DATA_IN	Input	No valid data on input
Z_IN(19:0)	Input	Real/Imaginary unfiltered Data In
RL_NIM	Input	Real/Imaginary Data In qualifier
Z_IN_NZ	Input	Non zero forced Data In value
Z_IN_VALID	Input	Data In valid, active high
MW_DVB-T/H_F Filter Core Outputs		
EMPTY_DATA	Output	No data valid on output
Z_OUT[13:0]	Output	Real/Imaginary filtered Data Out
RL_NIM_OUT	Output	Real/Imaginary Data Out qualifier
Z_OUT_NZ	Output	Non zero forced Data Out value
Z_OUT_VALID	Output	Data Out valid, active high

Critical Signal Descriptions

In a typical application the MW_DVB-T/H_F Filter Core directly interface with the upconverter and the same system clock signal serves to syncronize both the input of data to the upconverter and the MW_DVB-T/H_F logic. In order to ensure correct timing relationship (setup/hold time requirements) at the input of data to the upconverter an OFFSET timig constraint is detailed into the Xilinx User Constraint File.

Core Assumptions

CLK_X_8 and CLK_X_16 clock signals must be connected to respectively CLK0 and CLK2X Clock Outputs of a DCM (Xilinx Digital Clock Manager) unit driven by the available system clock signal.

Verification Methods

Complete functional and timing simulation has been performed on the core. VHDL Test Bench and Simulation Vectors used for verification are provided with the core.

Recommended Design Experience

Users should be familiar with VHDL entry, synthesis, simulation and Xilinx design flows.

Available Support Products

A complete ETSI EN 300 744 V1.5.1 (2004-11) compliant DVB-T/H high performances single chip applications is available from MindWay S.r.l., as DVB-T/H Modulator Core (MW_DVB-T/H_P), input functions ASI/SPI channel interface, PCR restamping, null packets removal/insertion (MW_DVB-T/H_A), additional signal processing functions (Linear and Non-Linear Precorrection) (MW_DVB-T/H_FP) or Single Frequency Network synchronization (SFN) (MW_DVB-T/H_S).

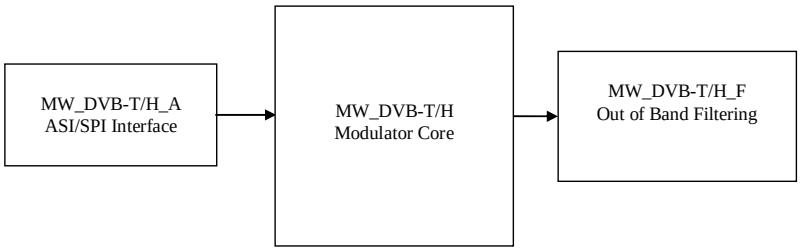
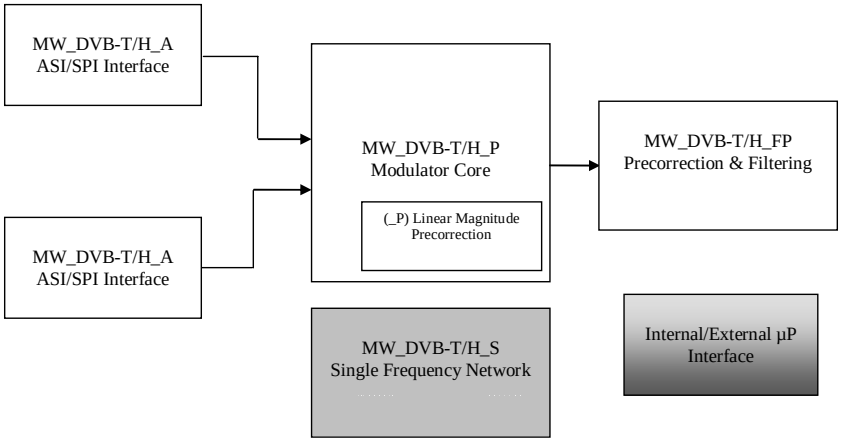


Figure 2: DVB-T Transmitter co-sited and operating on a channel adjacent to a transmitter for analogue television



Notes:

1) Linear Magnitude Precorrection functionality is implemented as part of the DVB-T/H Modulator Core (MW_DVB-T/H_P) because it processes OFDM symbol carriers before the IFFT block.

Figure 3: High-End DVB-T/H Transmitter

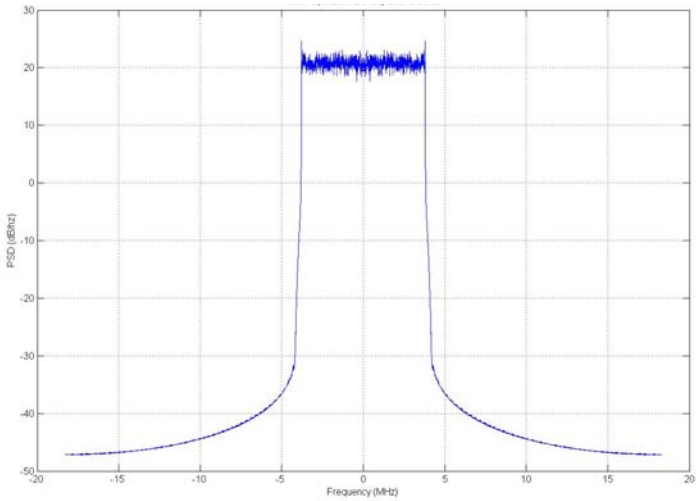


Figure43: MW_DVB-T/H_F Filter Core Output Spectral Density

Ordering Information

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Related Information

Industry Information (Optional)

ETSI EN 300 744 v1.5.1 (2004-11) Digital Video Broadcasting (DVB); Framing structure, channel coding and modulation for terrestrial television.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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